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By: Ken Dierberger

APPLICATION NOTE

A New Generation of Power MOSFET Offers Inproved Performance at Reduced Cost

A New Generation Of Power MOSFETs Offers Improved Performance At Reduced Cost

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ABSTRACT

In today's power electronic market place, as in other areas of electronics, reducing cost is necessary to stay competitive. A new generation of high voltage Power MOSFETs offers lower on-resistance ($R_{DS(ON)}$) using the same chip area as a previous generation of devices. Smaller die MOSFETs are also being produced with this technology that have the same $R_{DS(ON)}$ as a previous generation but now at a lower price.

This paper covers the use of these devices in a phase shifted control mode full bridge DC/DC converter featuring zero voltage switching. A comparison was made between the performance of an older generation device to the new generation device. The comparison shows that the new smaller die device, while providing reduced cost, produced equal performance to the older generation.

Introduction

Advances in resonant and quasi-resonant power conversion technology offer alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Presently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant and quasi-resonant technologies, primarily due to their lossless switching merits.

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by P. Vinciarelli [1]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters. In theory, the ON-OFF transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current switching, hence zero power switching. While true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin, significantly increasing conduction losses. In its OFF state, the switch returns to blocking a high voltage every cycle. When activated by the next drive pulse, the MOSFET output capacitance (C_{oss}) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique.

Zero Voltage Switching

Conventional zero voltage switching can best be defined as square wave power conversion during the switch's ON-time with "resonant" zero volt turn-ON switching transitions. For the most part, it can be considered as square wave power using either a constant OFF or ON time while varying the conversion frequency to maintain regulation of the output voltage Fixed frequency conversion using variable OFF and ON times can also be used to maintain regulation of the output voltage.

The benefits of lossless Zero Voltage Transition (ZVT) switching techniques are well known through the power supply industry.[2] The parasitic circuit elements can be used advantageously to facilitate resonant transitions rather than snubbing dissipatively. The resonant tank functions to put zero voltage across the switching devices prior to turn-ON, eliminating power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources gain significant improvements in efficiency with this technique. The full bridge topology as shown in Figure 1 will be the specific focus of this paper, with emphasis placed on the fixed frequency, phase shifted mode of operation.

Phase Shifted Control

The phase shifted mode H-bridge functions by applying two square waves to the primary of a transformer. For an output duty cycle of D=1 the two square waves would be 180 degrees out of phase as shown in Figure 2. For an output duty cycle of D<1 one of the square waves would be phase shifted resulting in the primary of the transformer being short circuited during a portion of the period, Figure 3.

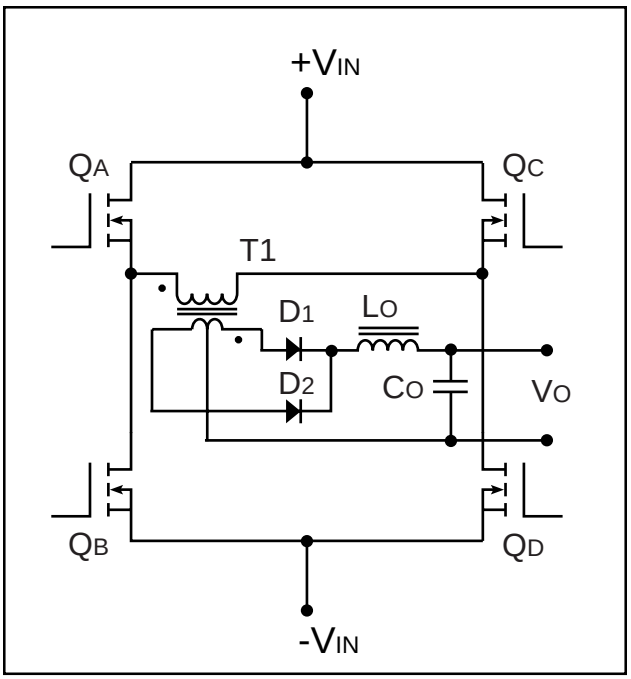

Figure 1. Full Bridge Topology.

A phase shifted mode power supply can be implemented using a conventional H-Bridge circuit, Figure 1. The switch drive signals are fixed frequency square waves with Q_A and Q_B switched 180 degrees out of phase and Q_C and Q_D switched 180 degrees out of phase. Using the switch drive signal of Q_A and Q_B as a reference, the switch drive signal of Q_C and Q_D will be phase shifted to create the duty cycle needed to produce the correct DC output.

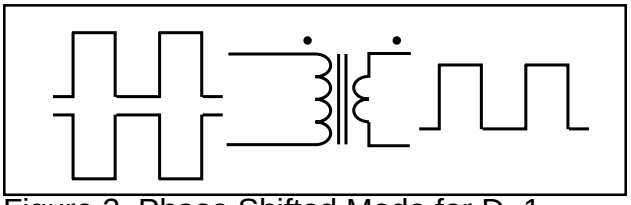

Figure 2. Phase Shifted Mode for D=1.

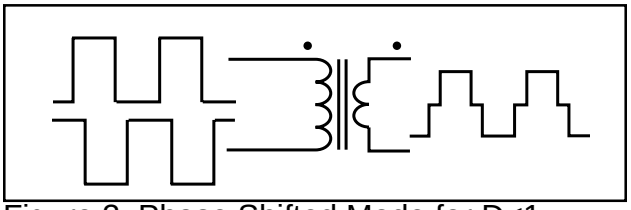

Figure 3. Phase Shifted Mode for D<1.

The gate drive signals for switch operation is shown in Figure 4. Interval 1, Q_A and Q_D are ON and Q_B and Q_C are OFF resulting in a positive voltage output from the transformer and transferring power to the inductor and the load. During interval 2, Q_C is switched ON and Q_D is switched OFF resulting in Q_A and Q_C shorting the primary of the transformer producing no output voltage and no power is delivered to the inductor from the power source. The inductor will free wheel during interval 2 and along with C_O will continue to deliver stored energy to the load. During interval 3, Q_A and Q_B are switched OFF and ON respectively resulting in a negative voltage being applied to the transformer. Again the power source will deliver power to the inductor and the load. The final interval 4, Q_C and Q_D are switched OFF and ON respectively resulting in a short across the transformer and no output voltage is produced. Again no power is delivered to the output and the inductor, along with C_O will continue to deliver stored energy to the load. The next interval 5, Q_A returns to ON and Q_B is returned to OFF. With Q_B and Q_C OFF and Q_A and Q_D ON this is the same conditions that existed in interval 1 and one cycle has been completed.

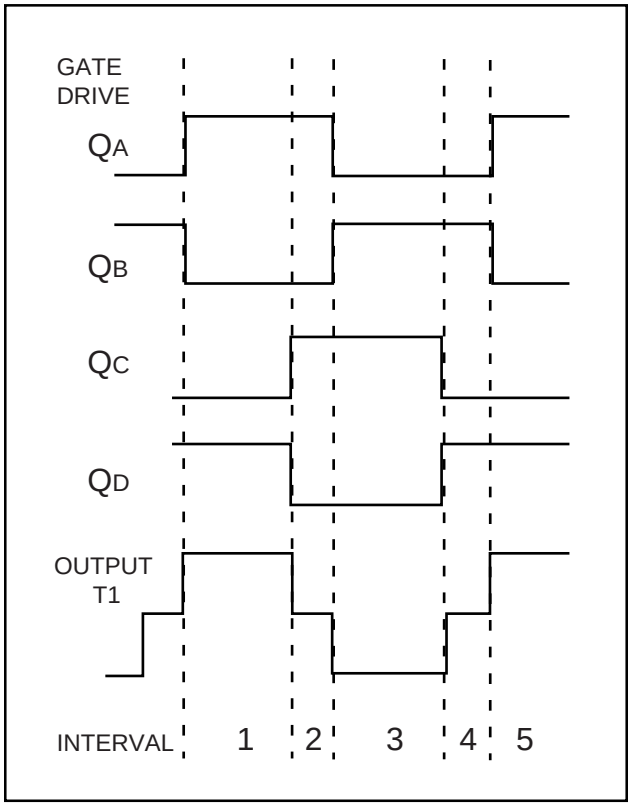

Figure 4. Gate Drive and T1 Output Signals.

It is noteworthy to point out that this circuit is hard switched and considerable power will be lost as a result of switching losses. The circuit, as described, will suffer from shoot-through current and resulting losses as Q_A-Q_B or Q_C-Q_D will most likely conduct current simultaneously during the transition between intervals.

One method commonly used to prevent shoot-through current power losses is to delay the turn-ON of one switch until the other switch in the leg has completely turned OFF. If we examine the use of this technique during the transition from interval 1 to 2 we note something interesting.

Zero Voltage Switched Phase Shifted Control

Figure 5 shows a MOSFET H-Bridge with output capacitances and intrinsic diodes included. Also shown as a separate component is the transformer leakage inductance L_R.

Examining the switching transition between intervals 1 and 2 in more detail, with a short delay added between the turn-OFF of Q_D and the turn-ON of Q_C, reveals it more than just limits the shoot-through current. When Q_D is turning OFF the voltage at the drain of Q_D will only rise as fast as the primary current of T_1 can charge the capacitance C_D, and discharge the capacitance C_C. If the turn-OFF speed of Q_D is much faster than the charge/discharge time of C_D/C_C the drain voltage of Q_D will remain low during turn-OFF and this will minimize the turn-OFF losses of Q_D. The drain voltage will continue to rise, but will not dissipate any power as energy is being stored in C_D and the energy stored in

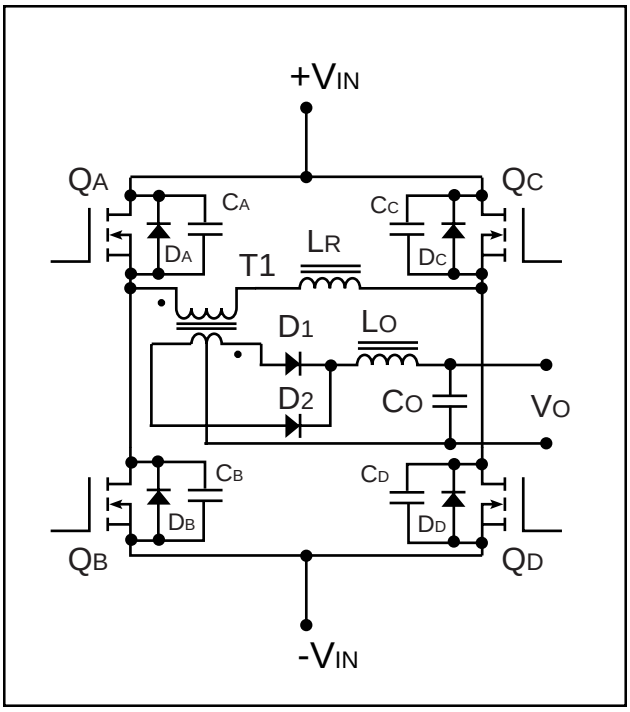

Figure 5. H-Bridge With Parasitic Diodes and Capacitances Shown.

C_C is returned to the input supply $+V_{IN}$, until it reaches a voltage slightly above the positive supply voltage ($+V_{IN}$). At this point the intrinsic diode D_C will begin to conduct clamping the drain voltage to V_{IN}. After D_C is conducting the voltage across the drain-source of Q_C is essentially zero and Q_C can be turned ON with a Zero Voltage Transition (ZVT) resulting in lossless switching. A MOSFET channel can conduct current in both forward and reverse directions and turning the MOSFET ON while the body diode is conducting will result in reducing the conduction losses of the diode.

The current driving the transition of the right leg can be approximated as the reflected load current in the primary of transformer T1 (I_P). During the right leg transition the current I_P will remain relatively constant as current will continue to flow through the output diode (D1) into the output inductor (L_O). The resulting right leg transition time is a linear ramp calculated from equation (1) :

$$I_P = C_R \frac{dv}{dt} \quad \text{or} \quad dt = C_R \frac{dv}{I_P} \qquad (1)$$

where:

I_P is the primary current of T1 at the end of interval 1

$dv=V_{IN}$

dt is the transition time

C_R is the effective value of C_C+C_D which is:

$$C_R = \frac{4}{3}\left(C_C + C_D\right) \qquad (2)$$

The 4/3 factor is used to estimate the average output capacitance over the drain voltage range.

At the end of the right leg transition the primary voltage of T1 will be zero as both Q_A and Q_C are conducting, resulting in a short circuit of the primary. With the primary of T1 at zero volts the secondary will also be at zero volts, stopping transfer of power to the output.

The presence of L_R in the primary circuit of T1 will steer the output current to continue to flow in D1 during the clamped freewheeling interval. Note that the current in the secondary windings never splits in half during the OFF period of power transfer as it does in a conventional, non-phase shifted H-bridge. During interval 2 the current in L_R will remain nearly constant as the current in L_O is still being reflected to the primary.

At the end of interval 2, Q_A will turn-OFF and Q_B will turn-ON, with a short delay added between the events. When Q_A is turning OFF the voltage at the source of Q_A will only drop as fast as the current supplied by L_R can charge C_A and discharge C_B. If the turn-OFF

speed of Q_A is much faster than the charge/discharge time of C_A/C_B the drain-source voltage of Q_A will remain low during turn-OFF and this will minimize the turn-OFF losses of Q_A. The source voltage will continue to drop until it reaches a voltage slightly below the supply voltage return ($-V_{IN}$). This transition will not result in any power dissipation as energy is being stored in C_A and the energy stored in C_B is returned to the input supply $+V_{IN}$. At this point the intrinsic diode D_B will begin to conduct clamping the drain voltage to $-V_{IN}$. After D_B is conducting the voltage across the drain-source of Q_B is essentially zero and Q_B can be turned ON with a Zero Voltage Transition (ZVT) resulting in lossless switching.

Note that the left leg transition is resonant and not linear like the right leg transition. As soon as the left leg transition begins the reflected output inductor disappears from the primary circuit. Reverse voltage being impressed on the primary of T_1 will begin the output diode commutation from D_1 to D_2 resulting in a short circuit of the secondary winding during the left leg transition thus removing the reflection of L_O from the primary circuit.

The left leg resonant transition must be fueled by energy stored in L_R. The exact circuit to describe this transition is a series L/C circuit with an initial current flowing equal to I_P at the start of the transition. L_R is the total series primary inductance and C_R is the effective circuit capacitance, $4/3(C_A+C_B)$. If the leakage inductance, L_R, of T_1 is too low and has insufficient energy to complete the resonant left leg transition a small inductor will need to be added in series with the primary of T_1. The primary current during this transition has a sinusoidal shape with the peak amplitude occurring at the beginning of the transition. Because of this, solving for the exact transition time will require taking the arcsin of the function describing the transition parameters at the beginning of the transition.

$$t_{TRAN(LEFT)} = \frac{1}{\omega_R} \arcsin \frac{V_{IN} Z_R}{I_P} \qquad (3)$$

Where Z_R is the resonant tank circuit impedance and ω_R is the resonant tank self oscillating frequency in radians:

$$Z_R = \sqrt{\frac{L_R}{C_R}} \qquad (4)$$

$$\omega_R = \frac{1}{\sqrt{L_R C_R}} \qquad (5)$$

At the end of the left leg transition T1 will have V_{IN} impressed across the primary as both Q_B and Q_C are conducting. With the primary of T1 at V_{IN} the secondary will be at V_{IN} multiplied by the turns ratio of T1, resuming transfer of power to the output.

At the end of interval 3 an identical analysis can be done to facilitate the transition from the conduction of Q_B and Q_C back to the conduction of Q_A and Q_D. The only difference is Q_C will be exchanged with Q_D and Q_B will be exchanged with Q_A in the discussion. The right leg will transition first in a linear mode as before and the left leg will transition second in a resonant mode as before. The shorted primary function will be done by the lower switches Q_B and Q_D.

A more detailed discussion of the preceding can be found in reference [2].

Evaluation Power Supply

To demonstrate the Phase Shifted ZVT Controlled Power Conversion technique we obtained an evaluation board from Unitrode Corp. which uses their UC3875 PWM controller IC. The evaluation board was

designed for 250 watts +12 to +32 volts output. Advanced Power Technology (APT) made some modifications to the evaluation power supply to convert it to 1000 watts at 48 volts output. Specifications for the power supply are:

V_{IN}	$400V_{DC}$
V_{OUT}	$48V_{DC}$
I_{OUT}	$20.5A_{DC}$
P_{OUT}	1000W
Efficiency	>93%

$400V_{DC}$ input voltage was chosen because this allows the power supply to be operated from a Power Factor Corrected (PFC) universal input (85 to $265V_{AC}$) preregulator. The $48V_{DC}$ output voltage was chosen to match the requirements of the telecom industry.

Design Overview

The circuit used for the evaluation power supply is shown in Figure 6 with the parts list shown in Appendix 1.

This design conforms in principle with the Unitrode application notes References [2, 3, 4]. Details of the differences between this design and the aforementioned application notes can be found in reference [5]. In summary the main differences in the evaluation power supply are: 1. The control circuitry is ground referenced to the output DC ground not the input DC ground. This improves the regulation of the output voltage and allows easier implementation of over current protection. 2. Coupling capacitors C1 and C2 are inserted in series with the driver transformers primary to improve the symmetry of the v-t product for the transformer cores and protects against saturation. A coupling capacitor C3 has been added in series with the power transformer T4 and has the same function as C1 and C2. 3. The v-t product can be asymmetrical if there are differences in coupling of both secondary halves to the primary, differences in the forward voltage between the rectifier diodes or by modulation of the error amplifiers output by clock-synchronous distortion. The disadvantages of this method are: The gate drive transformers may require additional insulation to meet safety standards. An isolated auxiliary power supply must be provided to power the UC3875. This is easily implemented if a PFC Preregulator is used to drive the converter.

Three major modifications made by APT to increase the evaluation power supply design to 1000W were: The main power transformer was changed back to a planar transformer similar to the design in reference [3]. APT30D20K diodes were used for the output rectifiers to accommodate the increased output current requirements. APT5020BNFR, APT5020BVFR and APT5017BVFR FREDFETs were all evaluated in the circuit. The APT5020BNFR, APT5020BVFR were found to provide equal performance. The APT5017BVFR showed a few tenths of a percent better efficiency. All devices offer low $R_{DS(ON)}$ to minimize conduction losses which are the dominant losses of the switching transistors. The APT5020BVFR is the better choice due to its lower price. The FREDFET was selected to provide better safety margin for commutative dv/dt of the body diode during no-load and short circuit operation of the power supply.[6]

Several minor modifications were needed to adjust the operation of the controller to accommodate the higher power and output voltage. The clock frequency was increased to 300KHz to provide a conversion frequency of 150KHz. The ramp and slope were adjusted for the new frequency. The current sense resistor was changed to 5 milliohms. The voltage divider for the error amplifier was adjusted for the 48V output voltage.

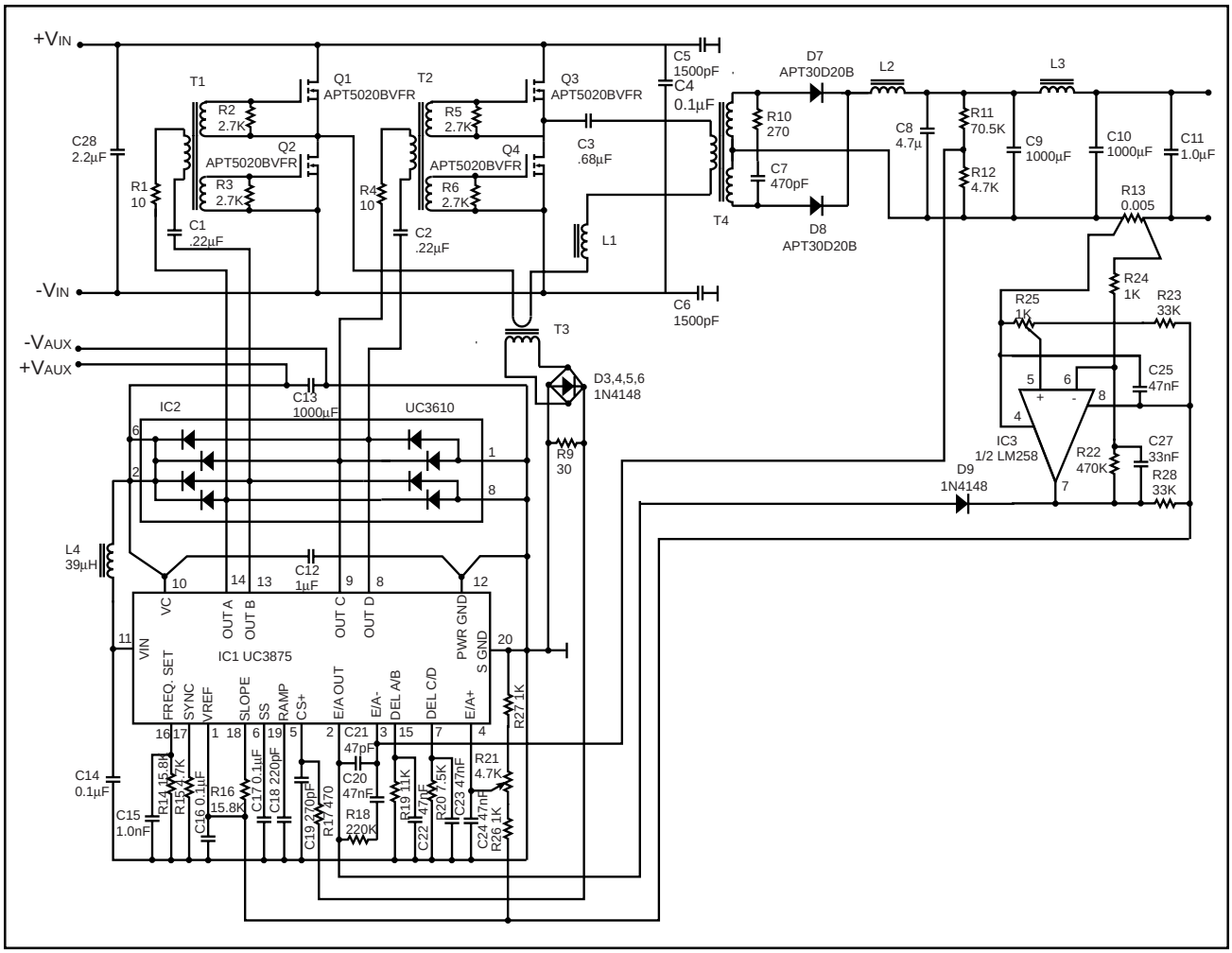

Figure 6. Schematic of the Evaluation Power Supply.

The power supply board layout is shown actual size in Figure 7. Note the small heat sinks required to cool the power MOSFETs. In fact the power dissipation of each FET is estimated to be under 2W at full load. A small fan was required to cool the power supply as the resonant inductor L1 was operating hot. Additional refinement of this component appears to be required. All other components were cool to the touch after several minutes of run time. The overheating of L1 prevented long run time testing. Once L1 is optimized it is believed that the better performance of the APT5017BVFR will be more significant and will make this device the better choice for the power supply. The parts list is given Appendix 1.

Performance

The evaluation power supply was tested over a load range of 100W to 1000W. The unit maintained ZVT to a load of under 50% and achieved an efficiency of over 93% from a load range of 750W to 1000W. Load regulation was ±0.18% from 100W to over 900W and was ±0.56% from 100W to 1000W. The loss of regulation above 900W was due to the required duty cycle reaching very near 100%. This could be corrected by an adjustment in the transformer turns ratio.

A graph of the measured converter efficiency is shown in Figure 8 for loads above 100W. Efficiency remains above 91% above 450W. The efficiency drops under 91% with

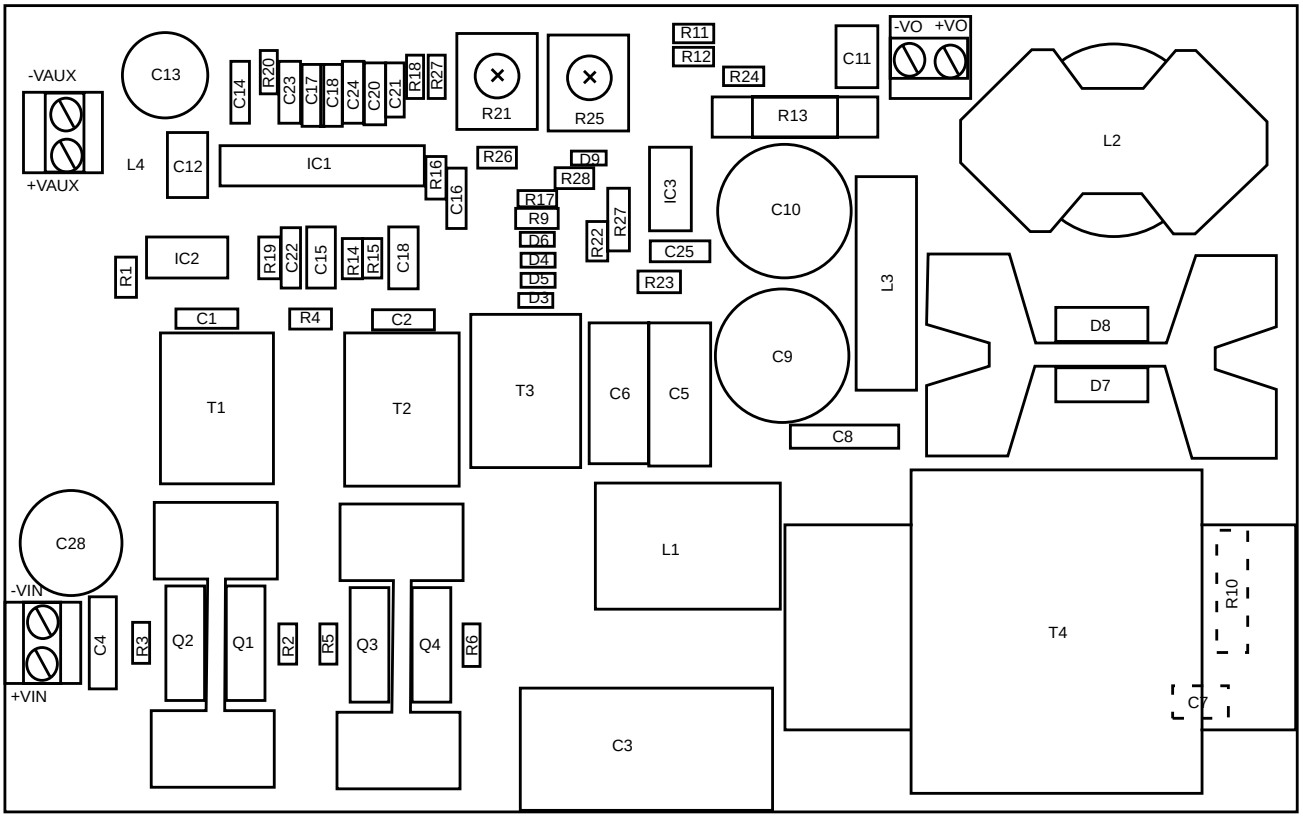

Figure 7. Power Supply Board Layout.

loads below 450W as the MOSFETs begins to hard switch for a portion of their switching transitions. The primary circulating current during the freewheeling interval is too low to discharge the resonant left leg capacitance to zero prior to turn-On and switching loss is incurred. At a slightly lighter load the same will hold true for the linear transition right leg.

Further design work could be done on the resonant inductor to lower it's losses. It seems to be the highest loss component in the unit. This would improve the efficiency of the unit over the entire operating range and especially at the high load end. Better optimization of its value could lower the point where hard switching begins thus improving the midrange efficiency. Be aware that this may also require other design tradeoffs which may adversely effect the operation of the power supply.

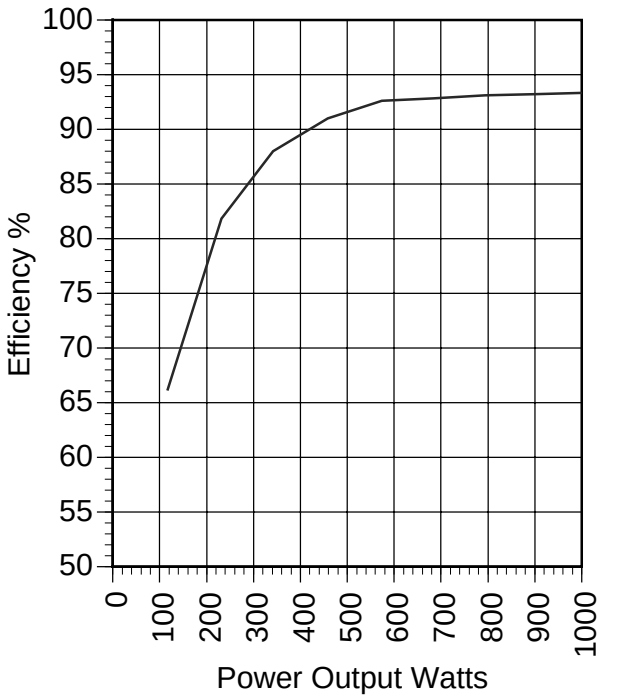

Figure 8. Converter Efficiency Versus Power.

Total power loss versus load is shown in Figure 9. This illustrates that non-ZVT operation is not the worst case for power dissipation in this design and full load is still the worst case. Therefore, operation under this lossy condition is acceptable from a thermal standpoint since ample cooling has been provided for much more power loss. Total losses range from about 46W at half load to 72W at full load and 60W at the 100W load. The increase in dissipation at the lower loads is the result of the loss of ZVT and the MOSFETs beginning to hard switch.

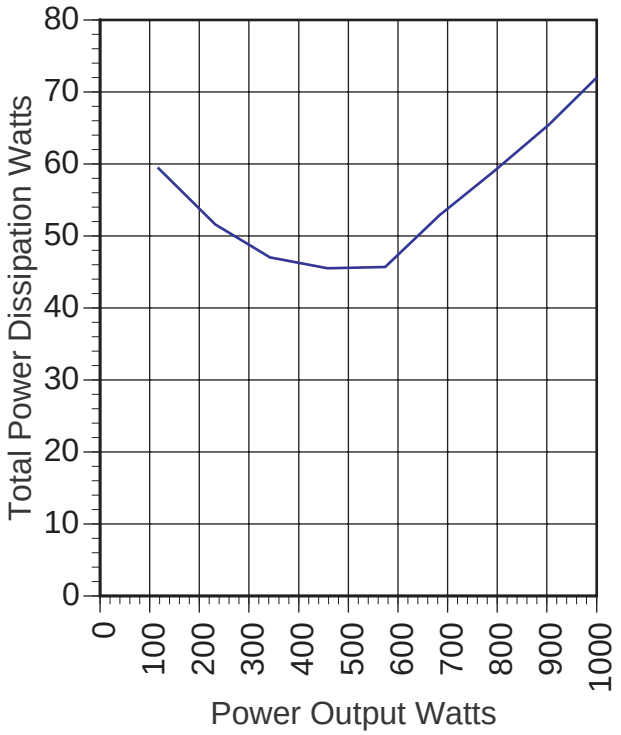

Figure 9. Total Power Dissipation versus Power Output.

Conclusions

This paper presented a typical application for the fixed frequency, phase shifted ZVT switchmode technique. Efficiency was shown to be very good and areas to improve the efficiency were noted. The very low power dissipation of the MOSFETs reduced the requirements for large heat sinks and will improve the reliability of the power supply. The use of the new generation of MOSFET from Advanced Power Technology reduced the cost of the power supply without sacrificing performance.

[1] P. Vinciarelli, “Forward Converter Switching At Zero Current,” U.S. Parent # 4,415,959 (1983)

[2] Bill Andreycak, “Designing a Phase Shifted Zero Voltage Transition (ZVT) Power Converter,” Unitrode Power Design Seminar SEM-900

[3] Bill Andreycak, “Design Review: 500 Watt, 40W/in3 Phase Shifted ZVT Power Converter,” Unitrode Power Design Seminar SEM-900

[4] Bill Andreycak, “Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller,” Unitrode Products & Applications Handbook 1995-96

[5] Bernd Ilchmann, “UC3875-Evaluation-Tool 250W DC/DC-Converter,” Unitrode-Application-Service

[6] A. Pietkiewicz and D. Tollik, “Operation of High Power Soft-Switched Phase-Shifted Full-Bridge DC-DC Converter Under Extreme Conditions,” IEEE 0-7803-2034-4/94, 1994

APPENDIX 1

EVALUATION POWER SUPPLY BOARD: PART LIST

	Part Number	Value	Rating	Remarks
1	C1	0.22µ	63V	MKT
2	C2	0.22µ	63V	MKT
3	C3	0.68µ	400V	Poly
4	C4	0.1µ	500V	X7R-Ceramic
5	C5	1500p	400 Vac/4KV	Class Y, Safety Type
6	C6	1500p	400 Vac/4KV	Class Y, Safety Type
7	C7	470p	400V	Ceramic
8	C8	4.7µ	100V	X7R-Ceramic
9	C9	1000µ	100V	Electrolytic
10	C10	1000µ	100V	Electrolytic
11	C11	1.0µ	63V	MKT
12	C12	1.0µ	63V	MKT
13	C12	1000µ	16V	Electrolytic
14	C14	0.1µ	63V	MKT
15	C15	1n	63V	MKT
16	C16	0.1µ	63V	MKT
17	C17	0.1µ	63V	MKT
18	C18	220p	63V	Ceramic
19	C19	270p	63V	Ceramic
20	C20	47n	63V	MKT
21	C21	47p	63V	Ceramic
22	C22	47n	63V	MKT
23	C23	47n	63V	MKT
24	C24	47n	63V	MKT
25	C25	47n	63V	MKT
27	C27	33n	63V	MKT
28	C28	2.2µ	400V	Electrolytic
31	D3	1N4148	75V/0,2A	Universal Diode, Low Power
32	D4	1N4148	75V/0,2A	Universal Diode, Low Power
33	D5	1N4148	75V/0,2A	Universal Diode, Low Power
34	D6	1N4148	75V/0,2A	Universal Diode, Low Power
35	D7	APT30D20B	200V/30A	APT
36	D8	APT30D20B	200V/30A	APT
37	D9	1N4148	75V/0,2A	Universal Diode, Low Power
38	IC1	UC3875	N-Package	Unitrode
39	IC2	UC3610	N-Package	Unitrode
40	IC3	LM258	P-DIP 8	National Semiconductor, Etc.
41	L1	33µH	3A	
42	L2	22µH	10A	
43	L3	3µH	10A	
44	L4	39µH	50mA	Small-Signal Choke
45	R1	10	0,25W	Metal-Film, Low Inductance
46	R2	2.7K	0,25W	Metal Film
47	R3	2.7K	0,25W	Metal Film
48	R4	10	0,25W	Metal-Film, Low Inductance
49	R5	2.7K	0,25W	Metal Film
50	R6	2.7K	0,25W	Metal Film
53	R9	30	0,25W	Metal-Film, Low Inductance
54	R10	270	2W	Metal-Film, Low Inductance
55	R11	70.5K	0,25W	Metal Film
56	R12	4.7K	0,25W	Metal Film
57	R13	0.005	20W	Metal-Band, Low Inductance
58	R14	15.8K	0,25W	Metal Film
59	R15	4.7K	0,25W	Metal Film
60	R16	15.8K	0,25W	Metal Film
61	R17	470	0,25W	Metal Film
62	R18	220K	0,25W	Metal Film
63	R19	11K	0,25W	Metal Film
64	R20	7.5K	0,25W	Metal Film
65	R21	4k7	0,25W	Trim-Resistor
66	R22	470K	0,25W	Metal Film
67	R23	33K	0,25W	Metal Film
68	R24	1.0K	0,25W	Metal Film
69	R25	1.0K	0,25W	Trin-Resistor
70	R26	1.0K	0,25W	Metal Film
71	R27	1.0K	0,25W	Metal Film
72	R28	33K	0,25W	Metal Film
73	Q1	APT5020BVFR	500V/0.2Ω	APT
74	Q2	APT5020BVFR	500V/0.2Ω	APT
75	Q3	APT5020BVFR	500V/0.2Ω	APT
76	Q4	APT5020BVFR	500V/0.2Ω	APT
77	TRF1	Driver-XFMR	3kV-Insul.	
78	TRF2	Driver-XFMR	3kV-Insul.	
79	TRF3	CS-XFMR	3kV-Insul.	
80	TRF4	PWR-XFMR	3kV-Insul.	

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