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By: Denis Grafham

APPLICATION NOTE

IMPROVED POWER MOSFETS BOOST EFFICIENCY IN A 3.5kW SINGLE PHASE PFC

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Abstract:
Minimum switching losses are essential for high efficiency in power conversion circuits operating at ultrasonic frequencies. Switching losses are minimized by reducing the "on-to-off" and "off-to-on" transition times of the powerMOSFET switches, thereby reducing those periods where high instantaneous currents and voltages occur simultaneously. This is achieved through innovative design of the MOSFETs themselves and by careful attention to the gate drive circuits. However, when lightning-fast turn-on provokes the hard commutation of associated diodes, as in continuous-mode boost converters configured for power factor correction, both turn-on losses in the MOSFET and unwanted EMI generated by diode recovery can rise uncontrollably unless ultra-low-stored-charge **F**ast **R**ecovery **E**pitaxial **D**iodes are used. Other factors influencing MOSFET switching losses include the amplitude of the currents and voltages being switched, the clock frequency, the ability of the drive circuit to rapidly charge and discharge MOSFET input and Miller capacitances, the effectiveness of the cooling system and the presence of any RC snubbers. Circuit considerations aside, the technology of the MOSFET itself is also fundamental for high efficiency, and in this context conduction as well as switching losses must be considered.

At high operating frequencies the average gate power needed to switch a large area PowerMOSFET is considerable. The drive circuit output impedance must be low to encourage rapid transfer of the gate charge Q_g, and by definition less Q_g translates to faster switching and a more economical driver. Low on-chip series gate resistance reduces the input time constants and encourages uniform switching across the chip. To shrink conduction losses $R_{DS(ON)}$ must also be low, but commensurate with the smallest possible chip for minimum cost and lowest output capacitance.

This paper charts the technological evolution of APT's powerMOSFETs from the earliest PowerMOS IV® designs to the latest PowerMOS 7™ products. The improvement in performance of a 3.5kW boost converter equipped in turn with different generation products is evaluated, as well as the influence of various MOSFET package styles on thermal behaviour and potentially harmful overvoltages.

Introduction:

The motivation for Power Factor Correction is the need for better utilization of power distribution systems through harmonic-content reduction. In North America and in Japan, as well as in other countries where the bulk of domestic electricity consumption is from 120 volt AC mains, loads presenting a poor power factor severely limit the real power that may be drawn from the mains. Although the problem is not as acute in Europe and in other regions where 230V single phase mains is the norm, the benefits of reduced line harmonics are still important. With this in mind, most countries in the European Union now enforce the provisions of IEC Directive 1003-2, limiting the allowable harmonic content in the mains for connected loads in excess of 250W. Such limits are low enough to make PFC obligatory for virtually all non-resistive loads, the most polluting of these being switch mode power supplies, or equipments containing them.

The boost converter topology illustrated in Figure 1 is that most often chosen for single phase PFC applications. Discontinuous-mode operation is very common in low power environments, but above about 750 W continuous-mode is almost universal. Here, peak currents are not so high, MOSFET turn-off losses are lower and output ripple at the PWM frequency is reduced. The downside is higher turn-on switching losses in the MOSFET and the possible generation of excessive EMI by reverse recovery of the boost diode[1, 2].

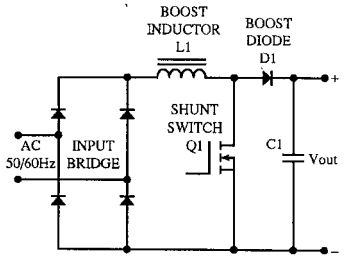


FIGURE 1. BOOST CONVERTER

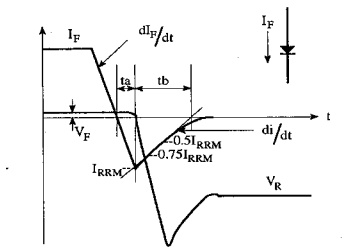


FIGURE 2.
DIODE REVERSE RECOVERY

Each time Q1 turns-on to divert inductor current from output to ground, the minority-carrier charge accumulated in D1 during conduction must be swept out by reverse current flow. While this current is

flowing, the diode behaves as an effective short circuit clamping the MOSFET drain to Vout. The MOSFET must then conduct the sum of diode-recovery and inductor currents at a drain potential of 390VDC until reverse recovery of D1 is complete. Very high turn-on switching losses are inevitable.

During the final phase of diode recovery, depicted in Figure 2, the reverse current decays from I_{RRM} to zero and reverse blocking capability is regained. The di/dt of this final ramp is determined primarily by the diode technology rather than by the circuit. If the diode is excessively " snappy", that is it recovers with too high a di/dt, the diode/ MOSFET/output capacitor loop may be shocked into very high frequency oscillations. Such ringing, whose energy content is directly related to I_{RRM}, generates unacceptable levels of EMI. In extreme cases, over voltages generated by "snap" interacting with stray circuit inductance may even destroy the FRED.

Fortunately, should such ill-effects occur, they are readily attenuated by slowing down the MOSFET at turn-on. Progressively softer dI_F/dts in Figure 2 produce ever lower I_{RRM}s, with less and less energy being stored for noise generation. Despite the longer turn-on times, MOSFET losses do not necessarily increase, at least initially, thanks to the lower peak currents it has to switch.

At MOSFET turn-off no such compromises are needed, in that the turn-on of D1 has little effect on the FET. Q1 should therefore be turned off as quickly as possible to minimize its own switching losses.

Boost Converter Test Assembly:

The 3.5kW continuous-mode PFC converter of Figure 3 was created by marrying a modified Unitrode UC3854 IC controller board[3,4,5] to a fan-cooled heat exchanger, on which were mounted a rectifier bridge and the MOSFET/FRED pair being evaluated, initially an ISOTOP® packaged APT 5010JVRU2 boost module. To minimize stray inductance, a second PCB bearing the filter capacitor was attached to the ISOTOP® with short copper straps. PWM frequency was 100kHz, nominal no-load output 390VDC.

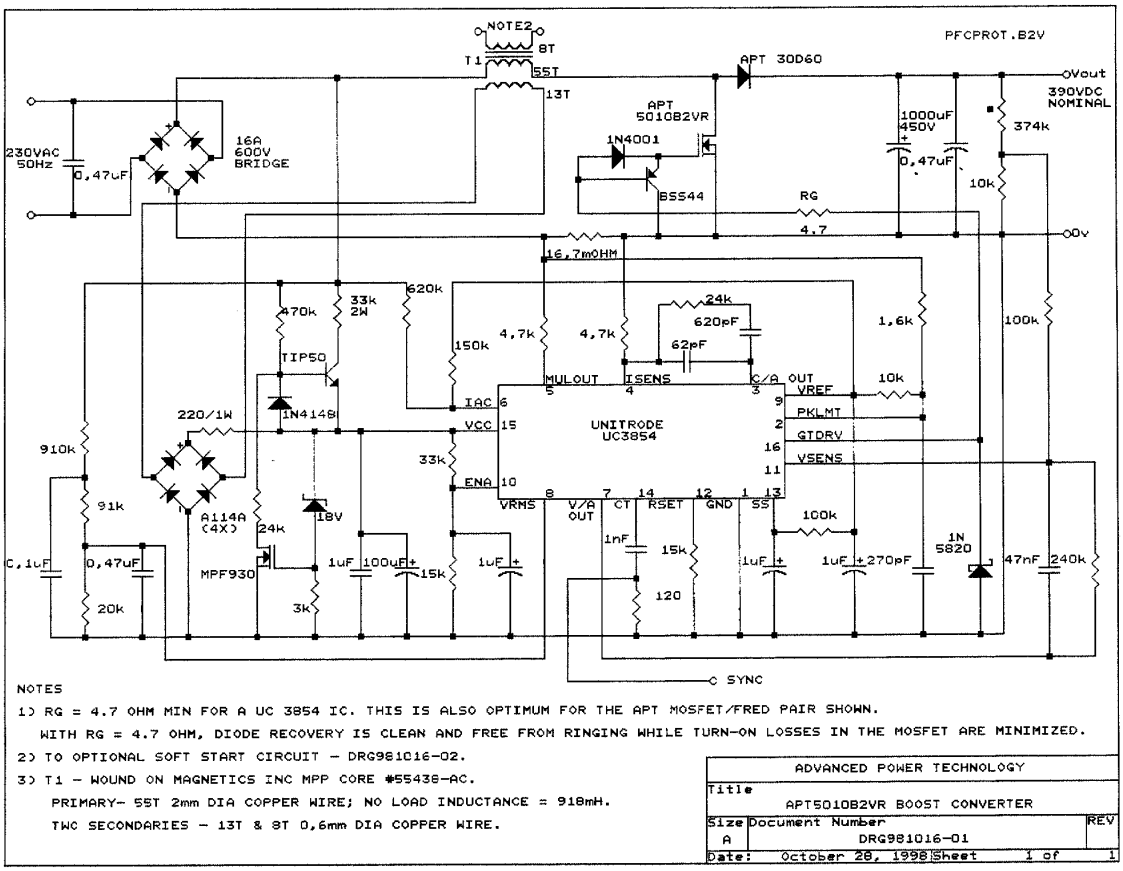
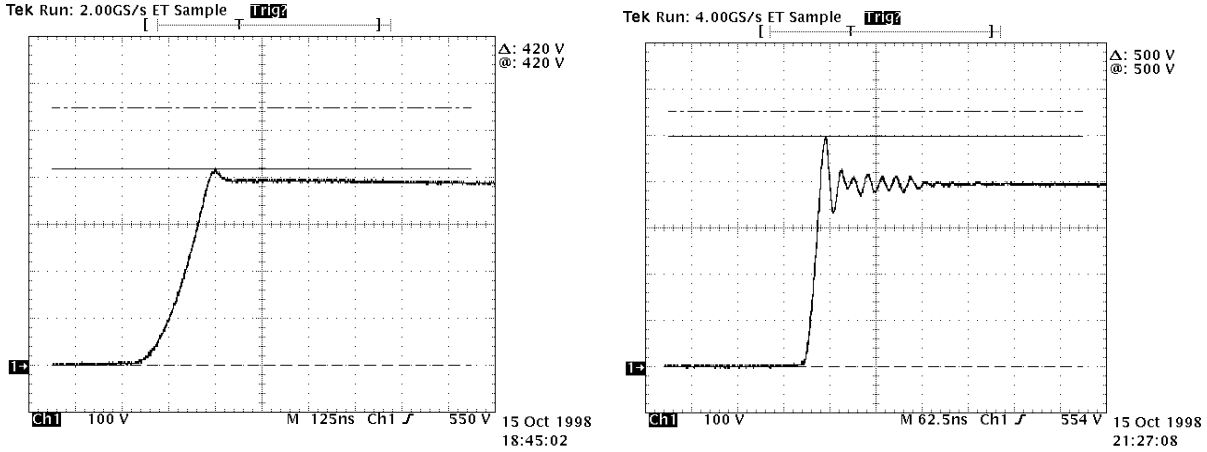


Figure 3 – Complete Boost Converter

Gate Drive Optimization:

One of the key benchmarks in PFC design is to establish optimum gate drive for the MOSFET during turn-on and turn-off. While it is well established that overlap between drain-current-fall and drain-voltage-rise times at turn-off is a major contributor to switching losses, it is also known that most controller ICs are incapable of discharging the gate capacitance and absorbing the Miller current of a large die MOSFET quickly enough to minimize overlap. In the circuit of Figure 3, the high-pulse-current PNP emitter follower connected between IC output and MOSFET gate effectively shorts the MOSFET gate to ground at turn-off, thereby eliminating this problem. Comparative measurements show that when the circuit is operated at 2kW without the emitter follower, drain overlap increases from 50ns to 150ns and semiconductor losses rise from 53W to 86W. These higher losses would likely precipitate thermal runaway were the circuit to be operated at 3.5kW, rendering the PNP obligatory at such power levels. Ironically, the much higher circuit di/dts produced by the emitter follower can also generate dangerously high voltage transients, unless great care is taken to minimize circuit stray inductance. MOSFET drain voltage and current waveforms with and without the PNP are illustrated in Figure 4.

References 1 and 2 show that for any given boost-diode technology there is a limited range of MOSFET turn-on di/dt that yields the best mix of low switching losses and near zero FRED-generated EMI. As already mentioned, at elevated di/dt, peak recovery currents in the FRED are very high, causing excessive switching losses in the MOSFET and exacerbating any tendancy for the FRED to "snap". Here, recovery current decays from its peak value to zero so fast that the entire circuit is shocked into oscillation. Should this occur, EMI becomes unmanageably high.



a) without emitter-follower b) with emitter-follower

Figure 4 – Drain-Source Voltage at turn-off

As the MOSFET is slowed down by gradually increasing R_G, peak recovery currents in the FRED diminish rapidly. Initially, the rate at which this occurs is high enough for losses in the MOSFET to actually decrease, despite the longer turn-on times. By the same token, any tendency for the circuit to ring is lessened. Eventually, though, the ever-longer MOSFET turn-on times predominate over the lower recovered energy in the FRED, and total losses begin to rise again. This indicates that there is a range of R_G values where MOSFET turn-on losses are at or near a minimum, with EMI noise very low or non-existent. It cannot be over-emphasized, however, that the values of R_G so identified apply only to a specific combination of MOSFET and FRED, and will also depend heavily on physical layout of the power circuit.

In a boost converter piloted by a UC3854, the risk that ringing between the MOSFET gate impedance and IC-driver produces dangerous voltages across the driver imposes a 4.7Ω minimum value on R_G[5]. Figure 5 illustrates the EMI-free nature of an APT5010B2VR PowerMOS V® turning-on into a 1500W load with a 4.7Ω gate resistor. Output must be limited to 1.5kW because the 2 ½" long drain lead extension needed for the current probe adds too much stray inductance for safe turn-off at full power.

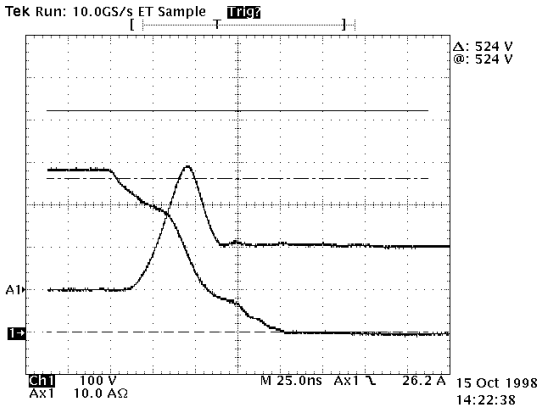


Figure 5 – MOSFET Turn-on, R_G = 4.7Ω (APT5010B2VR)

Voltage Overshoot at MOSFET Turn-off:

As emphasized already, fast MOSFET turn-off is highly desirable for best efficiency. With a PNP emitter follower, drain current transitions in the order of 1000A/µs are routine. While guaranteeing excellent efficiency, such transitions exacerbate the effect of parasitic strays in the critical MOSFET/FRED/output-capacitor loop. Assuming that the MOSFET will not be rated at more than 500V, based on a nominal 390VDC output, the available margin for voltage overshoots is just 110V. By Lenz' Law:

$$E = L_{STRAY} * di/dt.\ L = (110/1000) * 10^{-6}\ H = 110\mu H \text{ max.}$$

In conventional point-to-point PC board wiring, such low values of loop inductance are difficult to attain. Just a few centimetres of PC track are too much. Although inductive strays may be reduced somewhat by using stripline techniques, overshoots during steady-state operation at full output may still be dangerously high. Since physical layout is largely dictated by the size and location of the filter board relative to the semiconductors, a means must be found to non-inductively couple the two semiconductors together and then to non-inductively connect this pair to the capacitor. APT's ISOTOP® packaged PFC module is ideal for this purpose. 5-10nH chip-to-terminal strays facilitate low inductance internal connections, while top-surface terminals permit direct liaison to a double-side filter board via short straps. PFCs based on this concept can easily deliver the full 3.5kW allowed from European 230V/16A single phase mains without stressing the MOSFET beyond 500V during normal operation, although peak voltages may exceed this briefly at power-up. In the US, output power is limited to around 3.2kW by the 15ARMS fuses associated with 230V two-phase mains. When run from 115V single-phase mains, available power will be somewhat less than 1500W, because of increased circuit losses at low input voltages.

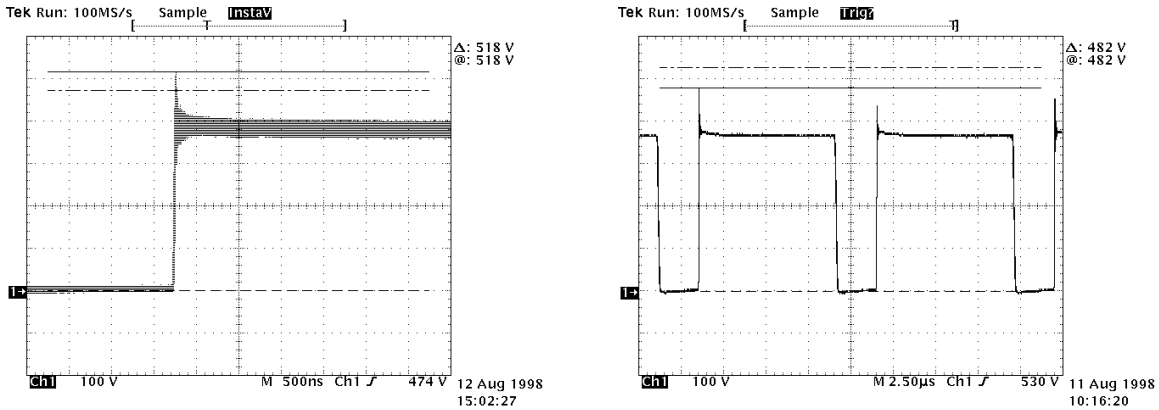
Circuit Performance:

1) The APT5010JVRU2 ISOTOP®-equipped test assembly was evaluated under the following conditions:

T_A = 27°C (after ½ hour run time), R_L = 39Ω (hot)

Recorded results were:

V_{AC} = 218VRMS (at bridge input), I_{AC} = 16.2ARMS,
V_{OUT} = 361VDC (361VRMS), T_{SINK} = 73°C



a) start-up b) steady-state

Figure 6 – Drain Voltage at MOSFET turn-off, APT5010JVRU2

From these data: $P_{OUT}=V_L^2/R_L=3342W$, $\Delta T_{SA}=46°C$

Losses in the PFC semiconductors:

$$P_{SC}=\Delta T_{SA} / R\theta_{SA}=46/0.36=128W$$

$$P_{IN}=(V_{AC} x\ I_{AC})=(218x16.2)=3532W$$

Soft start losses: P_{SS}=14 W at 16.2ARMS - from SC265 data sheet

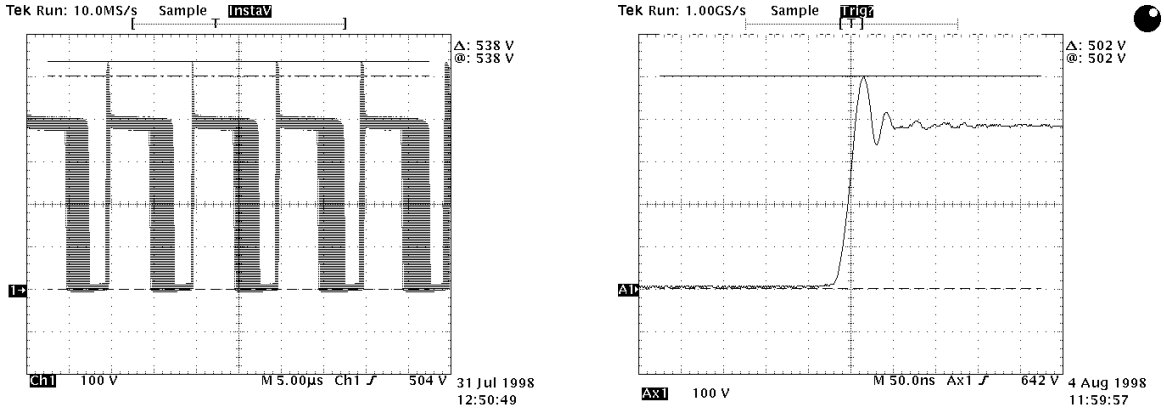
(the SC265 25ARMS triac based soft-start circuit is series with the AC mains is not shown on Figure 3)

Efficiency, excluding soft start losses:

$$\eta=P_{OUT}/(P_{IN}–P_{SS})=3342/ (3532 –14) = 95\%$$

As portrayed in Figures 6a and b, peak overshoot voltage at the MOSFET drain does slightly exceed 500V at start-up, but during normal operation stabilizes at a very safe 482V. In the unlikely event that startup transients ever drove the MOSFET briefly into avalanche, no harm would result as long as the total power rating of the device was respected. APT's Power MOS V® process is optimized to allow safe operation in repetitive avalanche.

2) The PFC test assembly was next evaluated with an APT5010LVR TO-264 packaged MOSFET and TO-247 packaged APT30D60B FRED replacing the ISOTOP®. The MOSFET was mounted in the same place as the module, the FRED alongside. Stray inductance in the MOSFET/FRED/filter capacitor loop was minimized by the use of superimposed copper stripline interconnects. Initially, a full-power 3.5kW run was made with the MOSFET attached to the heatsink with an M3 machine screw torqued to 6dNm, isolation being assured by a 0.6mm thick aluminium nitride shim. The FRED was similarly mounted, but with a Silpad rather than an AlN shim. Measured efficiency, at 94%, was almost identical to the ISOTOP®.



a) start-up b) steady-state

Figure 7 – Drain Voltage at turn-off, APT5010LVR

This is not surprising in that both products have the same MOSFET chips with similar junction-to-sink thermal resistances. The FRED is located on the sink close enough to the FET to ensure roughly the same heat distribution.

Overvoltage behaviour, however, is not at all comparable. Figures 7a and 7b depict MOSFET drain voltage waveforms at power-up and in the steady-state. Start-up transients peak at 538V instead of 518V, while the steady-state overshoots stabilize at 502V rather than 482V. As a consequence, the risk of repetitive avalanche during start-up, accompanied with high losses, is substantially increased. This situation is due entirely to the increased stray inductance.

3) The test assembly was next modified to allow spring-clip rather than M3 screw attachment of the TO-264 package. The clip applied a force of approximately 5kg between the FET and its sink, centred over the silicon chip. A full-load run was then made with the same conditions as before. The results were not as expected, in that the recorded heatsink temperature of 72°C was 3°C higher than before. Input and output voltages and currents were unchanged.

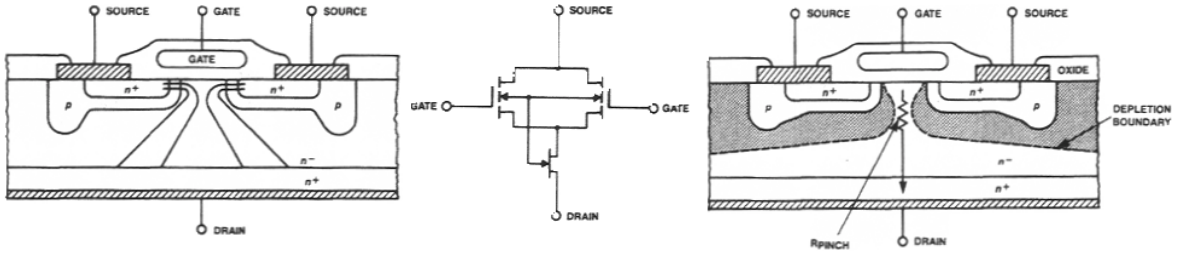
The most plausible explanation for this apparent increase in sink temperature is the improved thermal contact made possible by the clip. With a centrally located clip, good contact between semiconductor and sink is assured. With a screw, real contact is limited to a relatively small area around the screw. Further away, the contact degrades progressively due to package "tilting", this being exacerbated by the presence of any resilient isolating shim[6]. Because most of the heat is then transferred to the sink through a relatively

small area not directly under the heat source, case to sink thermal resistance is increased and the junction runs hotter. The lower measured sink temperature reflects poor heat transfer directly under the chip. Were the temperature probe closer to the screw, measured sink temperature would rise. Because higher junction temperatures cause increased losses and degraded reliability, clip mounting is to be preferred.

4) In a purpose-designed pressure-mounted package mounting holes are by definition superfluous, so their suppression results in smaller size, lower cost and improved performance for a given chip size. The T-MAX™ from APT is such a package, characterized by the same footprint as a TO-247 but accommodating the same chips as the larger TO-264. When evaluated in the PFC test circuit, a 5010B2VR T-MAX™ equivalent to the TO-264 5010LVR yielded substantially better results, equalling the 95% efficiency achieved by the top-of-the-line but more costly 5010JVRU2 ISOTOP.

PowerMOSFET Technology Evolution:

It is conventional wisdom that, in a multi-cellular powerMOSFET, the higher the number of unit cells in parallel per cm^2 of active area the lower will be the $R_{DS(ON)}$. The equivalent parameter in APT's interdigitated single cell topology is total channel length. In a high voltage powerMOSFET the major contributors to $R_{DS(ON)}$ are EPI-layer resistance, channel resistance and "ON" resistance of the parasitic JFET in series with the MOSFET drain. As shown in Figure 8, this JFET results from the physical relationship between adjacent p-well diffusions acting as gates that pinch-off current flow in its vertical descent to the backside drain.



a) source-to-drain current flow b) JFET orientation c) pinch off

Figure 8 - Parasitic JFET

Because EPI resistivity is directly proportional to breakdown voltage, the only way to decrease its effective resistance is to increase chip size. Channel resistance, on the other hand, is a direct function of the amount of channel per unit chip area, so adding more channel will reduce $R_{DS(ON)}$. A higher channel density, however, requires adjacent p-wells to be spaced closer together, which exacerbates the pinch-off effect. Eventually, at some level of packing density, the JFET resistance starts to increase faster than the channel resistance decreases, effectively limiting usable cell density. For a particular diffusion depth there is always an optimal channel packing density for minimum $R_{DS(ON)}$. Shallower diffusion depths allow a higher packing density. APT's PowerMOS V® technology, a cross section of which is illustrated in Figure 9, takes advantage of shallower junctions to increase the packing density compared to the earlier PowerMOS IV® design, also shown.

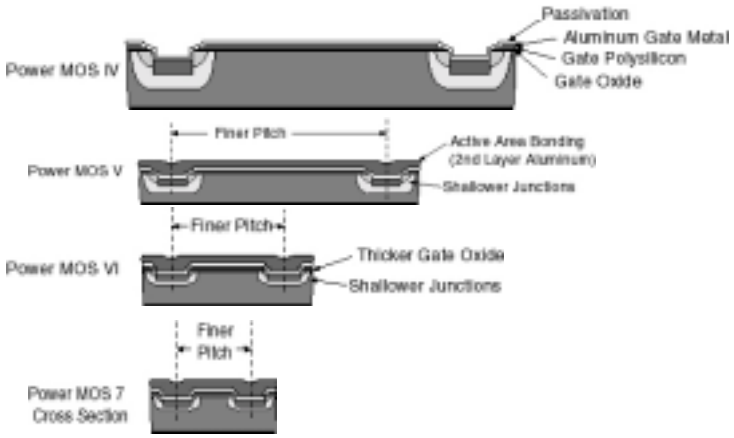


Figure 9 – Comparative Chip Topology

Another advantageous method to increase packing density, hence reduce total $R_{DS(ON)}$, is "over active area bonding". This technique, which eliminates previously unusable chip area underneath gate and source pads, allows wire bonding over active area by depositing a thick aluminium layer over the whole pre-passivated chip, thereby cushioning the impact of subsequent wire bonding operations. Openings etched in the passivation layers provide contact to the underlying gate and source metals. To ensure good contacts, these openings run the full length of the chip. As illustrated in Figure 9, "over active area bonding" is a standard feature of all APT PowerMOS V® and later topologies.

Whereas the combination of higher packing density and "over active area bonding" leads to lower $R_{DS(ON)}$, these factors do not materially improve switching performance, this latter being addressed by evolutionary changes in chip layout. By increasing the number of gate and source wires distributed across the chip, gate and source "finger" lengths are substantially reduced. More bond wires in parallel mean lower lead inductance, while more and shorter gate fingers mean lower lead resistance. The resulting lower input impedance, in conjunction with the input and reverse transfer Miller capacitances C_{gs} and C_{gd}, reduces both turn-on and turn-off delay times, More importantly, efficiency benefits from the faster rise and fall times resulting from the lower (Z_{in} x C_{gs}) time constant. Furthermore, less inductance in the source lead means less degenerative feedback to the gate signal, with beneficial effects on device gain and switching times.

With no noticeable slowdown in the trend towards higher SMPS switching frequencies, fuelled as always by the desire for smaller magnetics, the old adage that MOSFETs consume no gate power has long been discredited. In a switchmode application average gate power $P_g = (Q_g \times f_{sw})$, where Q_g is the total gate charge needed for turn-on. Although gate dissipation in the MOSFET itself is rarely a problem, the same cannot always be said for the driver, which must furnish the needed power. In many instances the gate driver is a low power IC feeding an array of several powerMOSFETs simultaneously, leading to unsustainable dissipation. To lower the power demands and limit driver cost escalation, for some time now circuit designers have been demanding new powerMOSFET devices with greatly reduced gate charge requirements. APT's recent PowerMOS VI™ technology was engineered to do just that.

By combining thicker gate oxide with shallower device junctions, both gate-input and reverse-transfer capacitances have been substantially lowered compared to the earlier PowerMOS V® designs, along with the gate charge that depends on them. Total gate charge has been slashed by up to 60%. The lower capacitances, together with reductions in parasitic series gate resistance made possible by tighter interdigitation, has enabled total switching times to be reduced by 50%. Shallower junctions permit tighter intergitation for the same JFET parasitic resistance.

Recently launched, APT's state-of-the-art PowerMOSFET 7™ product line incorporates newly available technology to minimize JFET resistance and to shrink chip size, while simultaneously improving thermal performance. Because the JFET is rendered less intrusive, interdigitation can be tightened for lower channel resistance and the gate structure enhanced through shorter finger lengths. For the same RDSon, chip sizes are much smaller and cost lowered. The normal downside to smaller chips, that is degraded junction-to-case thermal resistance, is compensated for by the use of thinned silicon chips. The thinning operation, which drastically reduces junction-to-case thermal resistance, is carried out on finished silicon wafers prior to dicing. Overall, this technology yields a much improved higher efficiency product characterized by more power in less space. At the time of writing (December 2000), APT's PowerMOS 7™ offers the best Figure of Merit ($R_{DS(ON)}$ x Q_g) of any conventional high power MOSFET in the whole industry.

Performance Comparisons:

To highlight the performance improvements brought about by successive generations of APT MOSFET devices, as a first step a TO264 packaged generation 5 APT5010LVR was compared against a PowerMOS IV® device with the same size chip. Driving a 3.3kW resistive load, measured overall efficiency was 94% for the APT5010LVR and 92% for the MOS IV device. Although this gain may appear modest from a system standpoint, the total reduction in power dissipation exceeded 20%, more than enough to justify a simplified and lower cost cooling system.

A further 19% reduction in losses was realized when a low gate charge APT5010LLC PowerMOS VI™ was substituted for the aforementioned MOS V device. In this case, even though the nominal $R_{DS(ON)}$s were the same, the smaller MOS VI chip bestowed both lower cost and enhanced performance, the latter due to the much faster rise and fall times.

Finally, an APT50M75LLL PowerMOS 7 with the same chip size as the original 5010LVR PowerMOS V® device was installed. Results were impressive, with additional 15% savings in losses recorded with respect to the MOS VI design.

Conclusions:

In the design of very high power PFC circuits the proper choice of power components, the optimization of MOSFET switching speeds and the mechanical layout of the output power loop are equally important to success. The selection of a low on-resistance MOSFET matched to a fast/soft-recovery FRED is the first step to achieving high efficiency with low EMI. The gate circuitry must then be tailored to drive the MOSFET/FRED pair for minimum switching losses and acceptable EMI. Finally, the MOSFET/ FRED/ output capacitor power loop must be laid out to minimize overshoot-producing stray inductance. It has been demonstrated that use of an ISOTOP®-packaged PFC module, incorporating APT's state-of-the-art Power MOS V® and FRED technologies, enables full authorized power to be drawn from either European (3500W) or North American (3200W) 230VAC mains at 95% efficiency, with safe snubberless operation of the power devices.

In situations where cost and/or mechanical considerations preclude use of a module, nearly the same performance is available from either a TO-264 or a T-MAX™ packaged MOSFET plus TO-247 discrete FRED. Should a TO-264 be preferred over the T-MAX™, it is shown that superior thermal performance is obtained by spring-clip mounting rather than with a screw. When either of these discrete products is paired with a FRED to replace the module, the unavoidable increase in stray inductance generates voltage overshoots across the MOSFET that just exceed 500V in the steady state, more during power-up. Because APT technology allows safe operation in avalanche, no harm will result as long as total power dissipation ratings are respected.

Insofar as choice of powerMOSFET technology is concerned, APT's latest PowerMOS 7™ design is a clear winner in terms of overall efficiency and "user friendliness". Combining very low on-state resistance with lightning-fast switching speeds and minimum gate charge requirements, chip thinning techniques ensure that thermal performance is not sacrificed to the altar of small chip size for lowest cost.

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