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APPLICATION NOTE

Improving the Full-bridge Phase-shift ZVT Converter for Failure-free Operation Under Extreme Conditions in Welding and Similar Applications

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Improving the Full-bridge Phase-shift ZVT Converter for Failure-free Operation Under Extreme Conditions in Welding and Similar Applications

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Abstract - **Most published material on the popular high power soft-switched full bridge phase-shift converter has focused on its use in telecommunications and similar power supply applications. In such service the load tends to be resistive and non-fluctuating in nature, so published literature, with one notable exception [1] has not probed the behavior of the topology under extreme conditions of near short-circuit or open-circuit load.**

In arc welding applications, it is relatively commonplace for the converter to function either with a very reduced load, during pauses between welds for example, or with a virtual short-circuit as when an electrode "sticks" to the work piece. This paper will identify a mechanism that induces power MOSFET failure when the converter operates into a short-circuit load, a condition that leads to the MOSFET being turned off while its own intrinsic diode is conducting reverse recovery current at the same time as normal channel current. The fast rising drain-source voltage ramp linked to this attempted turn-off can then induce second-breakdown in the parasitic NPN transistor associated with the MOSFET, in that the device is still full of minority carriers.

The physics of this operating mode will be examined in detail. Laboratory experiments described will establish a correlation between reverse recovery behavior of the intrinsic diode and converter immunity to failure. Circuit techniques to alleviate the failure-inducing stress will also be suggested.

I. INTRODUCTION

For some years now, high-frequency solid-state converters have been widely employed in the industrial arc welding field. The more than three orders of magnitude increase in operating frequency, from the 50/60Hz phase-controlled equipment of the sixties to the now commonplace 50-100kHz SMPS designs, has permitted substantial reductions in weight and size, enabling true welder portability to be achieved at very high power levels. Equally dramatic have been the advances made by the adoption of high frequency control for the arc welding process itself, with its complex mixture of heat input, material transfer, and difficult arc characteristics [2]. As an example, while the arc is being struck, despite a relatively low no-load source voltage of only 50V the initial arc current must be made to rise very rapidly. Thereafter, to assure properly controlled metal droplet transfer through the established arc, 1ms wide current pulses must be switched from 20A to 500A in less than 200μs, at a repetition rate of 200Hz.

Today, the most popular converter topology for use in electronically controlled arc welding is the half-bridge forward converter. To achieve the highest power levels, two such converters with their outputs phase shifted 180° apart may be connected in parallel across a common DC bus [3]. Hard-commutated IGBTs or power MOSFETs with passive dissipative snubbers are invariably specified as the power switches, depending on the mains voltage and output power range required. However, because switching losses in the semiconductors and companion snubbers limit the attainable frequency, these configurations are slowly being superseded by topologies based on resonant or similar soft-switching techniques. Because switching losses are theoretically non-existent in resonant or quasi-resonant converters, operational frequency is no longer limited by the semiconductors and may be increased substantially, with all the benefits in size, weight and control flexibility that result.

Great care must nevertheless be exercised in the choice of an appropriate soft-switching topology, in that the arc welding process itself imposes very stringent demands on the dynamic behavior of the welding source. The arc welding process is characterized by:

- A very wide load range, from open-circuit to short-circuit operation.
- A broad span of controlled load current, necessary to optimize the welding action.
- Extremely rapid load current changes.

These requirements dictate the choice of a topology capable of maintaining total or near total loss less switching, independent of load conditions. Most of the well-known resonant and soft-switching circuit arrangements leave much to be desired in this respect.

- Series resonant converters develop high turn-off losses when operating above resonance [4] [5]
- Quasi-resonant ZCS converters are intolerant of wide power variations, if switching losses are to be avoided [6].
- Multi-resonant ZCS and ZVT converters require costly and burdensome auxiliary circuits [8] [9].
- ZCS-PS-FB converters misbehave at low load current [7].

There is, however, at least one relatively simple topology that does satisfy the difficult demands of the arc welding industry, and that is the full-bridge phase-shift ZVT converter whose basic schematic is illustrated in Fig. 1. Note that the capacitor and diode shown in parallel with each MOSFET represent the parasitic output capacitance and drain-source diode of the MOSFET itself, and are not separate components. Also shown separately is the output transformer leakage inductance L_R. A slightly more complex variant of this topology also exists [10], where a saturable reactor and DC blocking capacitor are added in series with the transformer primary. This topology achieves ZVS conditions for one leg and ZCS conditions for the other.

II. FULL-BRIDGE PHASE-SHIFTED ZVT CONVERTER OPERATION

A. Zero Voltage Switched Phase Shifted Control

Conventional zero voltage switching can best be defined as square wave power conversion during the switch's ON-time, with "resonant" zero volt turn-ON switching transitions. For the most part, it can be considered as square wave power delivery using either constant OFF or ON time, while varying the conversion frequency to regulate the output voltage. Fixed frequency conversion, using variable OFF and ON times to modulate output voltage, is also quite common.

The benefits of loss less Zero Voltage Transition (ZVT), are well known in the power conversion world. Wherever possible, parasitic device elements associated with the semiconductors are used advantageously to facilitate resonant transitions, as opposed to resorting to dissipative snubbing as in hard switching. The resonant tank functions to put zero voltage across each switching device just prior to turn-ON, thereby eliminating power loss due to simultaneous voltage and current during the transition itself. High power converters operating from high voltage DC rails show significant improvements in efficiency with this technique.

The phase shifted H-bridge functions by applying two square waves to the primary of a transformer. For a duty cycle of D=1 the two square waves would be 180° out of phase as shown in Fig. 2. For a duty cycle of D<1 one of the square waves would be phase shifted, resulting in the transformer primary being short-circuited for a portion of the period, Fig. 3. The circuit is toggled by applying fixed frequency square wave drive signals to the MOSFET bridge, with M1 and M2 being switched 180° out of phase, M3 and M4 likewise. Using the drive signals of M1 and M2 as a reference, the drive signals of M3 and M4 are then phase shifted to create the duty cycle needed to produce the required output. The simplified gate signals needed to achieve this along with the resulting transformer primary voltage are depicted in Fig. 4. In reality, the absence of any "dead time" (time lapse) between the turn-OFF of one and the turn-ON of the other MOSFET in a given bridge leg as shown in Fig. 4, would lead to simultaneous conduction ("shoot-through")

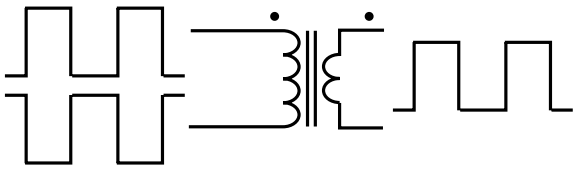

Fig. 2. Phase shifted mode for D=1.

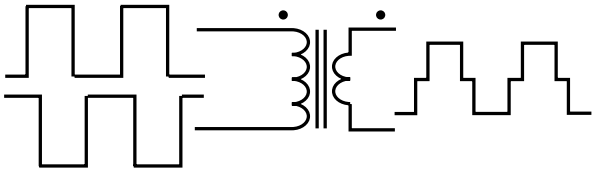

Fig. 3. Phase shifted mode for D<1

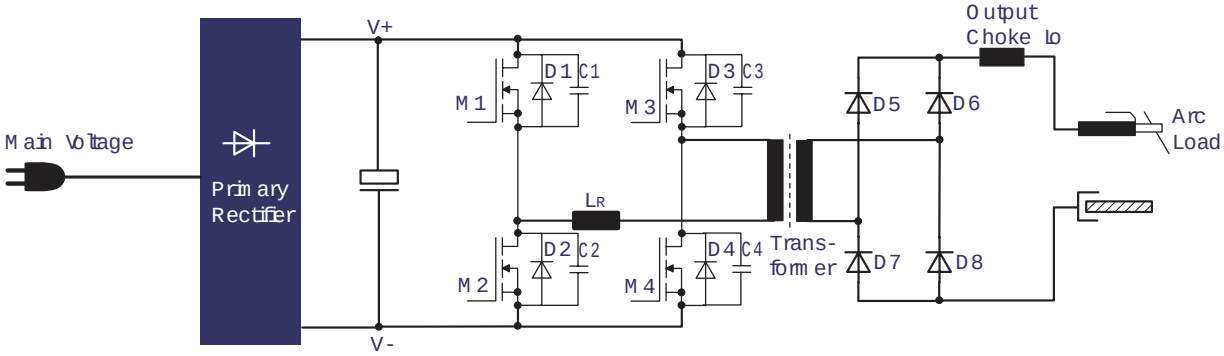

Fig. 1. Full bridge welding converter.

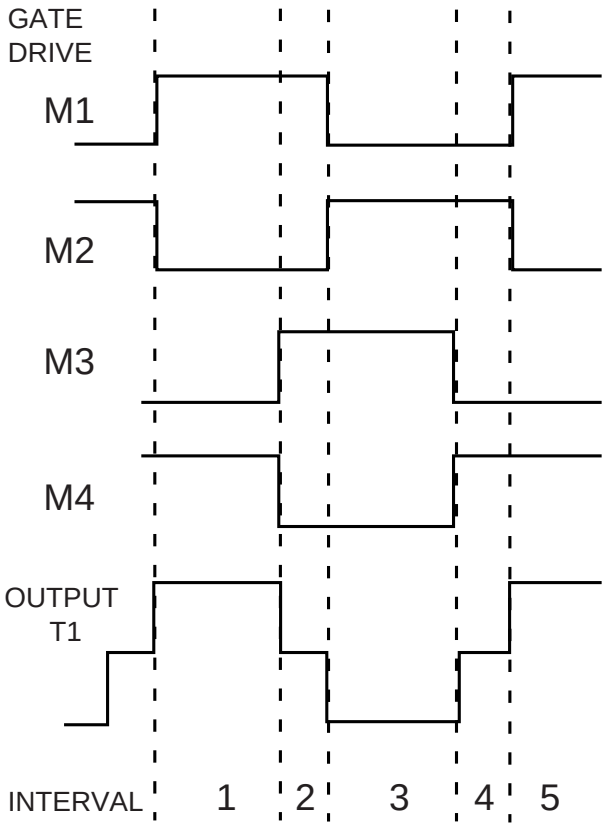

Fig. 4. Gate drive and T1 output voltage waveform.

at each transition point with enormous switching losses. Without dead time in fact, the circuit is unashamedly hard switched. The simple expedient used to prevent such shoot-through and convert the circuit into a soft-switching mode is to add dead time by slightly delaying the turn-ON of one switch until the other switch in the same leg has been completely turned OFF.

Referring to Figs. 1 and 4, in the modified circuit M1 and M4 are ON and M2 and M3 are OFF during interval 1, resulting in positive output from the transformer and power being delivered to the load. During the subsequent switching transition from interval 1 to 2 the effect of injected dead time now appears. Close scrutiny of this transition reveals that the delay does much more than just limit shoot-through. While M4 is turning OFF, its drain voltage can only rise as fast as the primary transformer current can charge C4 and discharge C3. If the turn-OFF speed of M4 is much faster than the charge/discharge time of C4/C3, the drain voltage of M4 will remain low during turn-OFF thereby minimizing M4's turn-OFF losses. The drain voltage will continue to rise, but power will not be dissipated as long as energy is being stored in C4 and returned to the DC rail from C3. When the drain voltage eventually reaches and then just exceeds V+, the intrinsic diode D3 will begin to conduct and clamp the drain voltage to V+. With D3 conducting, the drain-source voltage of M3 is virtually zero so this device can be turned ON with a Zero Volt Transition (ZVT) and loss less switching ensues. Since a MOSFET channel can conduct current in both directions, turning the MOSFET ON while its body diode conducts reduces conduction losses in the diode.

The current driving the right leg transition is approximately the reflected load current in the transformer primary, and this current will remain relatively constant, since the load current continues to flow through the output bridge and the smoothing choke L_0. The resulting right leg transition time is a linear ramp, given by:

$$I_P = C_R * dv/dt \quad (1)$$

or

$$dt = C_R * dv/I_P \quad (2)$$

Where I_p is the primary current in T1 at the end of interval 1, $dv = V_{IN}$, dt is the transition time and C_R the effective value of (C3 + C4).

At the end of the right leg transition the transformer voltage will be zero, as both M1 and M3 are both conducting to effectively short-circuit the primary. With T1's primary short-circuited its secondary will also be at zero volts, interrupting transfer of power to the load from the primary side. Load current is then sustained during the clamped freewheeling interval 2 by the energy stored in L_0 circulating through the bridge diodes D5/D8. Because L_0 is relatively large, load current is virtually constant during this period.

At the end of interval 2, M1 will turn-OFF and M2 will turn-ON with a short delay between these events as before. A sequence of events then takes place similar to those occurring during the right leg transition, with low loss turn-OFF of M1 and ZVT turn-ON of M2.

Note, however, that the left leg transition is resonant and not linear like the right leg transition. During left leg transition, because the transformer secondary is still short-circuited by the freewheeling bridge the impedance of L_0 cannot be reflected into the primary circuit. Under these circumstances the transition must be fueled by the energy stored in L_R alone. The exact circuit describing this transition is a series L/C loop with an initial current equal to I_P. L_R is the total series primary inductance and C_R is the effective circuit capacitance, slightly more than (C1+C2). If the leakage inductance L_R of T1 is too low to store enough energy to complete the resonant left leg transition, a small supplemental inductor must be added in series with the primary of T1. The primary current during this transition is sinusoidal in form, with its peak amplitude occurring at the start. Resonant tank self-oscillating frequency ω_R is given by:

$$\omega_R = 1/ (L_R * C_R)^{1/2} \quad \text{radians} \quad (3)$$

and Z_R, the tank impedance, is given by:

$$Z_R = (L_R/C_R)^{1/2} \quad \text{ohms} \quad (4)$$

At the end of the left leg transition, T1 will have V+ impressed across its primary, as both M2 and M3 conduct to

allow power transfer to resume. At the end of interval 3 an identical analysis facilitates the transition from the conduction of M2 and M3 back to the conduction of M1 and M4. The right leg will transition first in a linear mode, followed by the left leg in resonant mode as before.

A more detailed description of circuit operation may be found in [11].

B. Short-circuit Behavior

In a full-bridge ZVT switched PWM phase-shift converter, when the load is short-circuited the controller tries to limit output current by reducing the switching duty cycle. Such a situation occurs frequently in a welding converter every time the mobile electrode inadvertently "sticks" to the work piece. The attempt to limit current manifests as a drastically reduced phase shift between the two halves of the bridge, since active power is only delivered to the load during the phase shifted intervals. In this short-circuit mode, the time lapse between successive voltage transitions may be as brief as 300 - 600ns and the time available for body diode commutation no more than half this.

Referring to Figs. 5 and 6, prior to time t1 M4 and its associated body diode D4 conduct in parallel along with M2. Note that as long as the gate of M4 is forward biased with respect to its source, M4 is able to conduct drain current of either polarity. Simultaneous diode/channel conduction reduces losses through better silicon utilization. During this period there is no net voltage across the transformer primary so no power is delivered to the load. At t1 M2 is turned OFF, when the primary current is diverted to discharge C1 and charge C2 before transferring to M1/D1 in parallel at t2. During the interval t2 to t3 reactive energy stored in the primary leakage inductance is returned to the DC bus through M1/D1 and the still conducting M4/D4. At t3 the current changes polarity, now flowing positively through M1 and M4 instead of negatively through its channel/body diode. During the interval t3 to t4 positive bus voltage is connected across the transformer and power is delivered to the load. However, because the controller is trying to limit power under the prevailing short circuit conditions, this time interval can be very brief, in the order of 100 - 300ns, until at t4 M4 is turned OFF. Unless the MOSFETs are specified as fast-recovery FREDFET types, such a short time is grossly inadequate for complete recombination of the minority car-

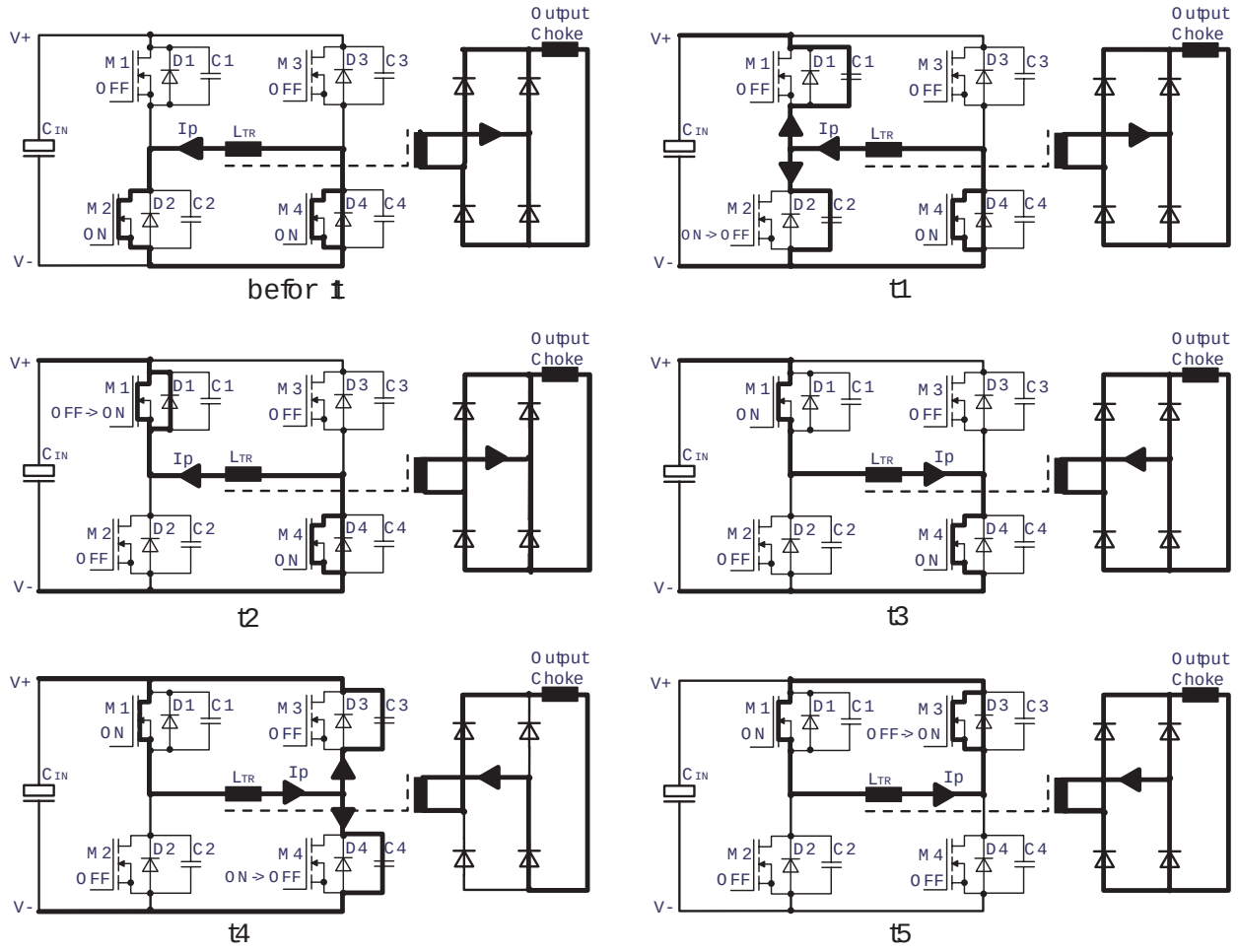

Fig. 5. Evolution of transformer current with time.

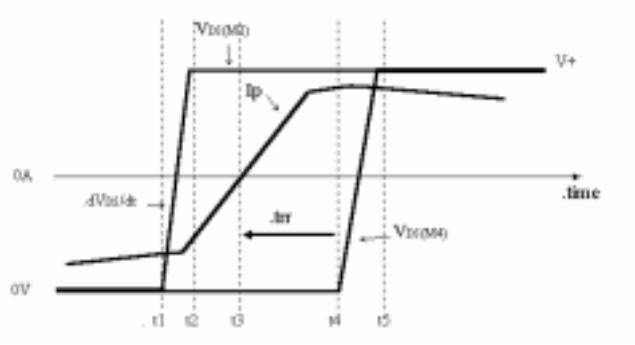

Fig. 6. Switch voltage and primary current relationship.

rier charge stored during diode conduction. In this event the presence of substantial charge in M4/D4 at turn-OFF together with a reapplied dv/dt that may exceed 12V/ns can precipitate destructive second breakdown of the parasitic NPN bipolar transistor present in all vertical MOSFET structures. The onset of such a phenomenon is clearly visible during the rise of drain-source voltage $V_{DS(M4)}$ (b) in Fig. 7. Here, the time lapse between the zero current crossover of Ip (b) and the reapplied voltage is only 150ns. Incipient failure is flagged by the relatively slow rise of drain voltage accompanied by high frequency ringing and a sudden rise in current signaling the MOSFET's reluctance to accept full blocking voltage. When reducing the time lapse further exacerbates this condition, the MOSFET eventually fails. This is portrayed in Fig. 8. If on the other hand the time interval t3 to t4 is extended to about 300ns, as represented by the waveforms of Ip (a) and $V_{DS(M4)}$ (a) in Fig. 7, operation is trouble free with a clean sharp rise of reapplied voltage, no ringing and no sudden increase in current. Such trouble-free turn-OFF is only possible when power MOSFETs incorporating fast recovery intrinsic diodes (FREDFETs) are specified.

In that a key contributory mechanism to failure is the injection of excess minority carriers initiated by dv/dt induced C_{CB} coupled parasitic transistor conduction, it should

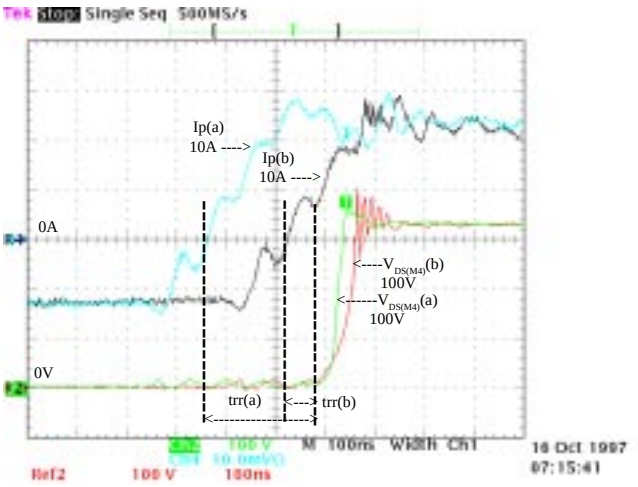

Fig. 7. Onset of MOSFET failure with short-circuit load

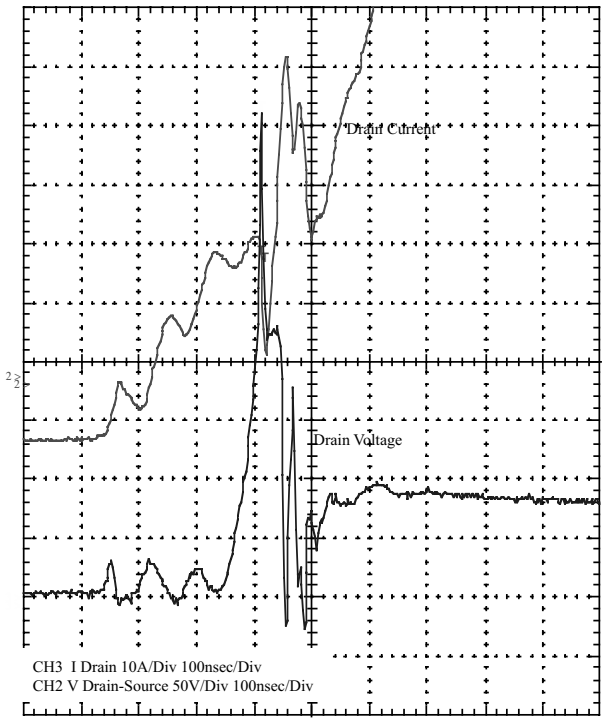

Fig. 8. MOSFET failure with short circuit load

be possible to retard the onset of failure by slowing down reapplied dv/dt. That such is the case is evidenced by the waveforms of Fig. 9, depicting circuit response when the MOSFET's own drain-source capacitance is augmented by connecting a discrete capacitor in parallel. Here, the waveforms are devoid of any trace of incipient failure even when the time between current zero and the onset of voltage is less

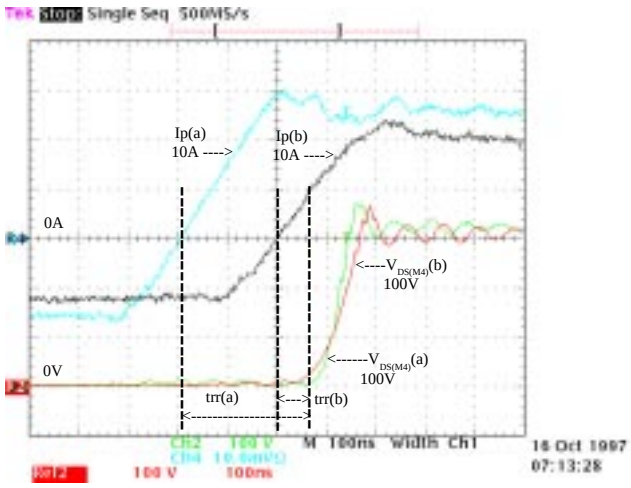

Fig. 9. Effect of additional capacitance with short-circuit load

than 100ns. Unlike the situation in hard-switched converters where adding snubber capacitance increases turn-ON losses, this supplementary energy is returned to the DC bus in the case of a ZVT converter. The downside of extra capacitance is that hard switching may result when the converter functions at very low load. In this situation, the energy stored in the transformer primary leakage inductance L_R may be insufficient to fully charge/discharge the capacitors, so ZVT transitioning is lost.

III. FAILURE MECHANISM THEORY

A. Body Diode Description

All Power MOSFETs have an intrinsic bipolar transistor in their structure. The vertical DMOS device, as illustrated in Fig. 10, has the base-emitter junction of the bipolar transistor shorted by the source metallization, forming the "Body Diode". If this parasitic bipolar transistor becomes active, the classic mechanism of second breakdown with current hogging can occur. This causes local heating, thereby increasing bipolar gain, further constricting current thus leading to device failure. If the Body Diode conducts in the forward direction, minority carriers remaining in the base region during diode recovery can cause transistor action with destructive results.

B. Body Diode Operation in a ZVT Circuit

It seems to be a common belief that a Zero Voltage Transition (ZVT) topology, where the MOSFET is turned ON while the Body Diode is conducting, the Body Diode will not be subject to second breakdown as current is reversed for a period of time during the cycle which should be long enough for the diode to recover. The reality is charge will remain stored in the Body Diode for a period of time much longer than the data sheet value for reverse recovery time or until high voltage is applied which will sweep the minority carriers out of the junction. Therefore, when reverse high voltage is applied to the Body Diode second breakdown maystill occur even after a relatively long time has passed.

In a typical ZVT topology forward current is forced into the Body Diode to clamp the output to either the positive or negative rail. This forward current causes the generation of minority carriers in both the P-Body and N-epi regions (Fig. 11).

Next the MOSFET channel is turned ON which diverts a portion of the current through the channel away from the Body Diode. A MOSFET can conduct current in both directions. The diversion of current away from the Body Diode will reduce the generation of minority carriers but will not stop it (fig. 12).

Next the external circuitry reverses the current flow through the device. This causes a small amount of reverse current flow in the Body Diode. The reverse current is small due to the very weak voltage field created by the low voltage generated by current flow in the low resistance of the channel. As a result some minority carriers will be swept across the junction removing them from the junction (fig. 13). After a short time enough carriers will have been removed enabling the junction to block a small amount of voltage. At this time the current is completely diverted to the channel. The Body Diode will no longer undergo forced recovery. Some carriers will continue to be eliminated by the normal recombination process. A large number of minority carriers remain in the junction for a considerable time (fig. 14).

When the channel is turned OFF the MOSFET will begin to block voltage imposing a higher reverse voltage on the Body Diode. The application of high reverse voltage on the Body Diode will sweep the remaining carriers across the junction (fig. 15). If the reverse current builds to a magnitude sufficient to activate the intrinsic bipolar transistor second breakdown may occur destroying the MOSFET.

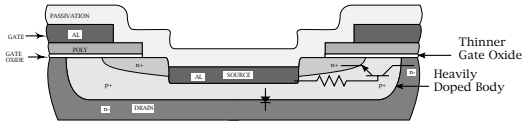

Fig. 10. Vertical DMOS cross-section.

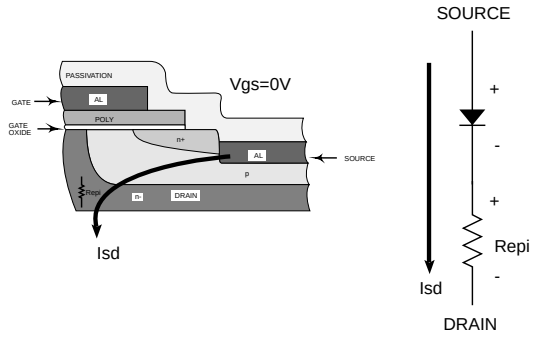

Fig. 11. Forward current flow in the Body Diode.

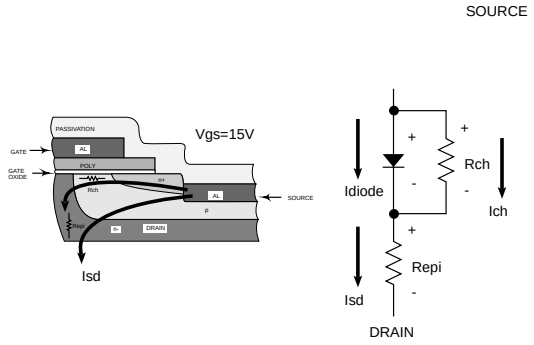

Fig. 12. Forward current flow in the Body Diode and the channel

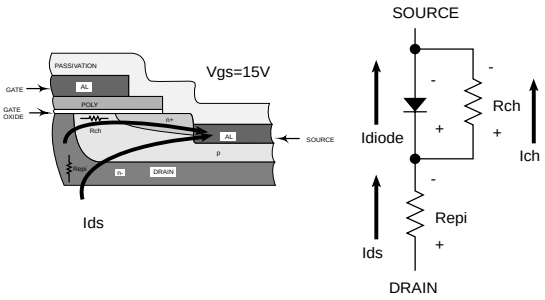

Fig. 13. Reverse current flow in the Body Diode and the channel.

IV. TEST VERIFICATION

A. Test Circuit

To evaluate this theory a test circuit was constructed which would force forward current into the Body Diode. Then stop the current flow without applying reverse voltage to the junction. After a measured period of time reverse voltage would be applied across the Body Diode junction and the remaining reverse recovery charge would be measured. The channel of the Device Under Test (DUT) could be turned ON or OFF at anytime before or during the test cycle. See abbreviated schematic Fig. 16.

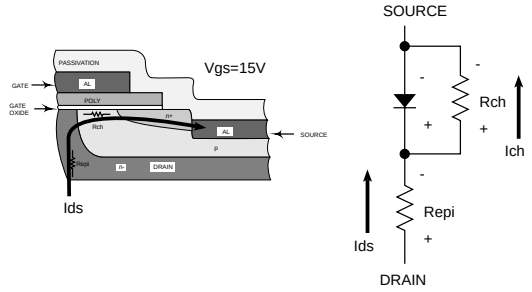

Fig. 14. Reverse current flow in the channel only.

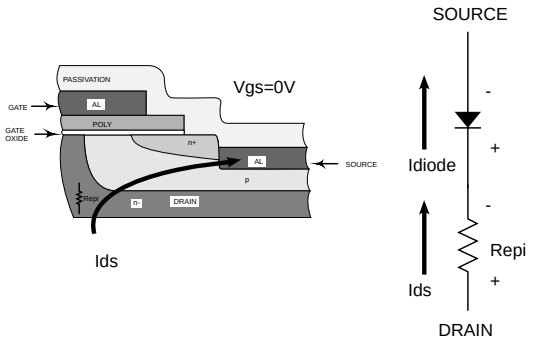

Fig. 15. Reverse current flow in the Body Diode only.

B. Stored Charge Remaining in the Junction, No Channel ON

A test was conducted without forcing forward current into the Body Diode and applying a reverse voltage of 800V at a dv/dt of 1.33V/nsec to determine the capacitance portion of the of the reverse recovery charge. This is defined as the baseline charge or the amount of charge that represents zero stored charge resulting from forward current flow.

A series of tests were conducted to determine the amount of time required, after the forward current was stopped, for all of the stored charge in the junction to be recombined.

The channel remained OFF during these tests. These tests were conducted forcing 5A of forward current for 10µsec and applying a reverse voltage of 800V at a dv/dt of 1.33V/nsec. The reverse voltage was first applied at 100nsec after the forward current was turned OFF. The test was repeated, applying the reverse voltage at a later time, until the baseline reverse recovery charge was reached. These tests were conducted on an APT10026JN, a standard MOSFET and on an APT10026JVFR, a fast recovery diode FREDFET. The results are shown in Fig. 17. It is clear from Fig 17 that there is charge remaining in the junction for a period of time longer than the reverse recovery specification would indicate. The standard MOSFET was near full recovery at 100µsec but it took until 200µsec to fully recover the device. The FREDFET was near full recovery at 3µsec and was fully recovered in less than 10µsec. The FREDFET recovered much faster then the standard MOSFET due to shorter minority carrier lifetime resulting in faster minority carrier recombination.

C. Stored Charge Remaining in the Junction, Channel ON

Another series of tests were conducted to determine the effect on stored charge by turning the DUT channel ON before and during the forward conduction period. The stored charge was measured 1µsec after the forward current was stopped. As before these tests were conducted forcing 5A of forward current for 10µsec and applying a reverse voltage of 800V at a dv/dt of 1.33V/nsec. The reverse voltage was applied at 1µsec after the forward current was turned OFF.

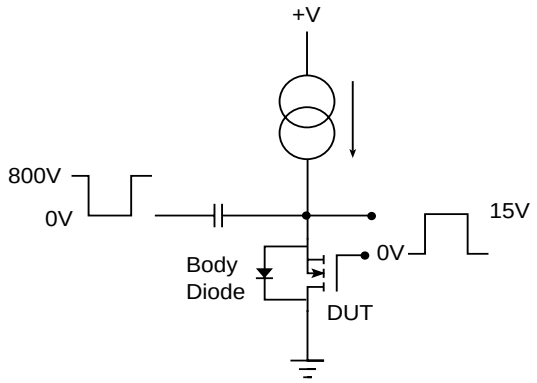

Fig. 16. Abbreviated schematic.

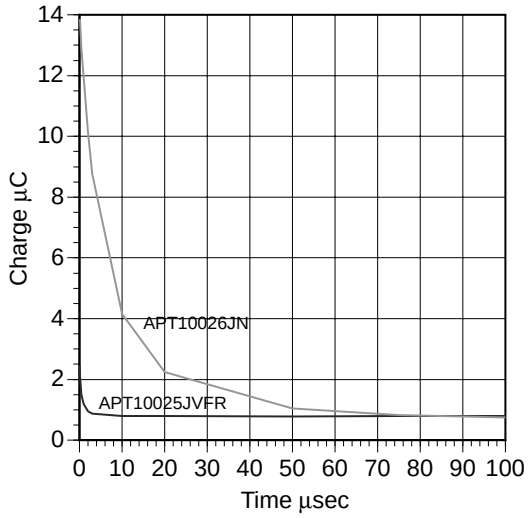

Fig. 17. Stored charge remaining in junction after forward current equals zero.

The first measurement was taken with the channel OFF. The second measurement was taken with the channel being turned ON 1µsec before the forward current was turned OFF and turned OFF 300nsec before the reverse voltage was applied. Subsequent measurements were taken by increasing the channel ON time by 1µsec steps and turning the channel OFF at 300nsec before the reverse voltage was applied. The results are shown in Fig 18. It is clear from Fig 18 that turning the channel ON during the forward conduction of the Body Diode will reduce the amount of stored charge and the sooner the channel is turned ON the less the remaining charge is. However, the standard MOSFET never reaches zero stored charge even when the channel is turned ON before the Body Diode conducts. The FREFET on the other hand, due to the short minority carrier lifetime, is virtually at zero stored charge when the channel is turned ON only during the last µsec of the of Body Diode conduction.

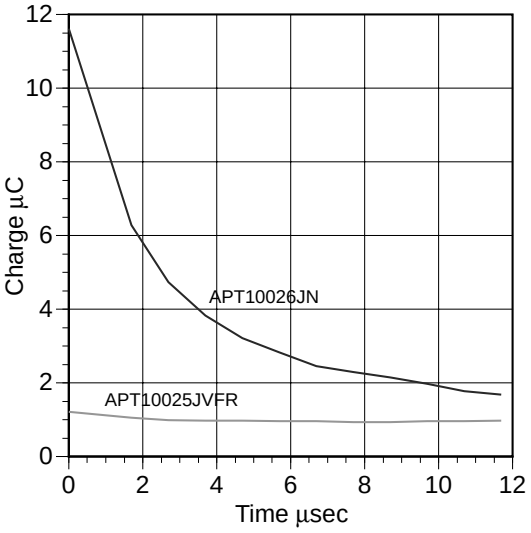

Fig 18. Stored charge remaining in junction versus channel ON time.

III. CONCLUSIONS

The requirement to use FREDFETs, fast recovery body-diode type MOSFETs, to insure reliable operation of phase-shift ZVT full-bridge converters has long been established. However, it has been demonstrated that under extreme operating conditions of near short circuit the ruggedness of the FREDFET may not be adequate to survive. The very fast commutation time from forward conduction of the body diode to forward conduction of the MOSFET channel coupled with a very short period to where the device is required to block voltage does not allow enough time for the body diode to clear of minority carriers. The resulting very fast dv/dt of about 12V/nsec was shown to initiate second breakdown of the intrinsic bipolar transistor causing failure of the MOSFET.

The addition of a capacitor in parallel with the drain-source of the MOSFET will slow the dv/dt to an acceptable value where the MOSFET will survive. The addition of these capacitors does not result in any degradation in efficiency at heavy loads but does cause a loss of efficiency at light loads. The increased power dissipation at light loads is not a problem as the maximum power losses still occur at full load and no redesign of the thermal management systems are required.

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