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APPLICATION NOTE

OPTIMIZING THE DESIGN OF 3.5KW SINGLE-MOSFET POWER FACTOR CORRECTORS

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Abstract:

At power levels exceeding about 750 Watts the most common power factor correction (PFC) topology in use today is the continuous-mode boost converter. In such a converter the gate drive output from popular IC controller chips is ill-suited for switching large area MOSFETs, and must be customized for lowest power losses and minimum EMI. The reverse recovery characteristics of the boost-diode strongly influence this process. In addition, the power circuit must be carefully laid-out for minimum stray inductance to inhibit the generation of dangerous over-voltages.

A key component for high power PFC design is APT's ISOTOP®- packaged boost module. In this product, the MOSFET and diode chips are mounted side-by-side beneath the main power terminals for lowest stray inductance. Superior thermal performance allied to VDE/UL recognized isolation is assured through use of an internal metallized ceramic substrate. APT's Power MOS V® process assures outputs of up to 3500W from 230V 50/60Hz mains at 95% or better efficiency.

Where cost or other considerations rule out an ISOTOP®, nearly equal performance may be obtained from either a TO-264 or T-MAX™ packaged MOSFET paired with a TO-247 FRED on a common heatsink, each with an insulating substrate.

This paper will define MOSFET gate drive requirements for minimum power losses and lowest EMI, evaluate the layout techniques necessary to limit turn-off voltage overshoots, and provide comparative data on package and mountdown options able to deliver up to 3500W power output from 230V 50/60Hz AC mains.

Introduction:

The motivation for Power Factor Correction is the need for better utilization of power distribution systems through harmonic-content reduction. In North America and in Japan, as well as in other countries where the bulk of domestic electricity consumption is from 120 volt AC mains, loads presenting a poor power factor severely limit the real power that may be drawn from the mains. Although the problem is not as acute in Europe and in other regions where 230V single phase mains is the norm, the benefits of reduced line harmonics are still important. With this in mind, most countries in the European Union now enforce the provisions of IEC Directive 1003-2, limiting the allowable harmonic content in the mains for connected loads in excess of 250W. Such limits are low enough to make PFC obligatory for virtually all non-resistive loads, the most polluting of these being switch mode power supplies, or equipments containing them.

The boost converter topology illustrated in Figure 1 is that most often chosen for single phase PFC applications. Discontinuous-mode operation is very common in low power

environments, but above about 750 W continuous-mode is almost universal. Here, peak currents are not so high, MOSFET turn-off losses are lower and output ripple at the PWM frequency is reduced. The downside is higher turn-on switching losses in the MOSFET and the possible generation of excessive EMI by reverse recovery of the boost diode [1,2].
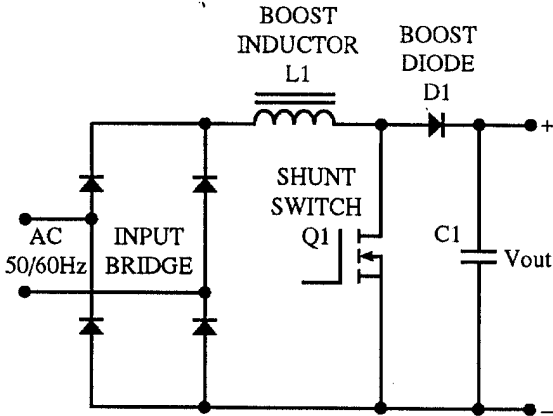

FIGURE 1. BOOST CONVERTER

Each time Q1 turns-on to divert inductor current from output to ground, the minority-carrier charge accumulated in D1 during conduction must be swept out by reverse current flow. While this current is flowing, the diode behaves as an effective short circuit clamping the MOSFET drain to Vout. The MOSFET must then conduct the sum of diode-recovery and inductor currents at a drain potential of 390VDC until reverse recovery of D1 is complete. Very high turn-on switching losses are inevitable.

During the last phase of diode recovery, depicted in Figure 2, the reverse current eventually falls from its peak I_{RRM} value to zero and reverse blocking capability is regained. The di/dt of this final ramp is determined primarily by the diode's own characteristics rather than by the circuit. If the diode is excessively " snappy", that is it recovers with too high a di/dt, the diode/ MOSFET/output capacitor loop may be shocked into very high frequency oscillations.

Such ringing, whose energy content is directly related to I_{RRM}, then generates unacceptable levels of EMI. In extreme cases, over voltages generated by "snap" interacting with stray circuit inductance may even destroy the FRED (Fast Recovery Epitaxial Diode).
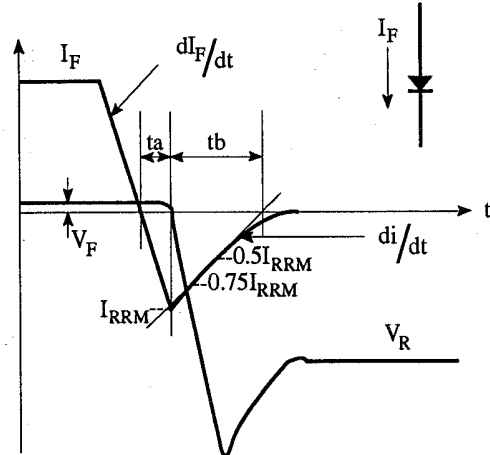

FIGURE 2.
DIODE REVERSE RECOVERY

Fortunately, should such ill-effects occur, they may be eliminated by slowing down the MOSFET at turn-on. Progressively softer dI_F/dts in Figure 2 produce ever lower $I_{RRM}s$, with less and less energy being stored for noise generation. Despite the longer turn-on times, MOSFET losses do not necessarily increase, at least initially, thanks to the lower peak currents it has to switch.

At MOSFET turn-off no such compromises are needed, in that the turn-on of D1 has little effect on the FET. Q1 should therefore be turned off as quickly as possible to minimize its own switching losses. APT's Power MOS V® products are ideal for these sockets, thanks to their exceedingly fast switching.

Boost Converter Test Assembly:

The 3500W continuous-mode boost converter test assembly illustrated in Figure 3 was created by marrying a suitably modified Unitrode UC3854 IC controller board to a fan cooled

heat exchanger, on which were mounted all the power semiconductors. To minimize stray inductance, a second PC board accommodating the filter capacitor was strapped to the APT ISOTOP® boost module with the shortest possible interconnects. The complete converter schematic is shown in Figure 4, while

References 3, 4 and 5 cover all aspects of circuit design. PWM frequency is 100kHz, nominal no-load output voltage 390VDC.

To prevent filter capacitor inrush current from arbitrarily tripping the mains circuit breaker during power- up, it was found necessary to
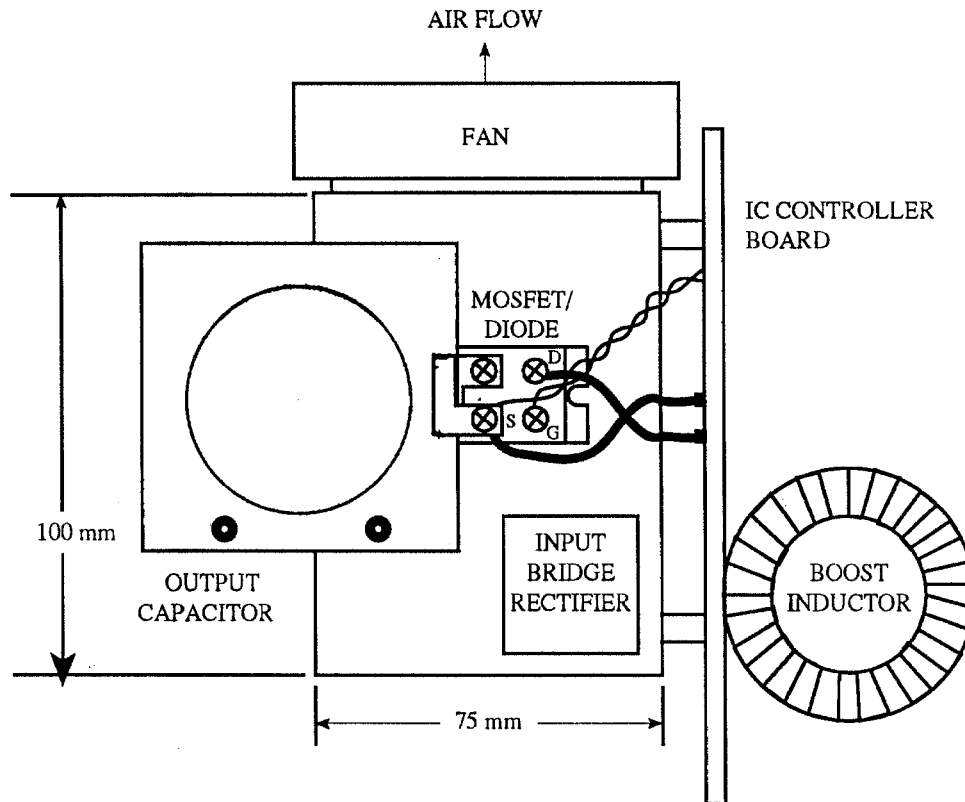
AIR FLOW

FIGURE 3. BOOST CONVERTER TEST ASSEMBLY

add the soft-start arrangement of Figure 5. In this circuit the triac is mounted on its own heat exchanger, with losses separated from the PFC proper.

Heat Exchanger thermal calibration:

The prime sources of heat in a PFC are the input rectifier, power MOSFET and boost diode. These are mounted on one face of a 10cm x 6.5cm x 7cm sunburst heat exchanger, cooled by an end-mounted axial extractor fan. The plastic-encapsulated rectifier bridge is rated at

26A/600V, and this is complemented by a single APT5010JVRU2 ISOTOP® containing MOSFET and FRED chips. Both modules are screwed down onto the heatsink with Thermalcote II non-silicone grease interfaces. A 1/8" Φ hole drilled through the heat exchanger web under the ISOTOP®'s baseplate accommodates the tip of a platinum resistance temperature probe, placed to measure sink temperature at its hottest point.
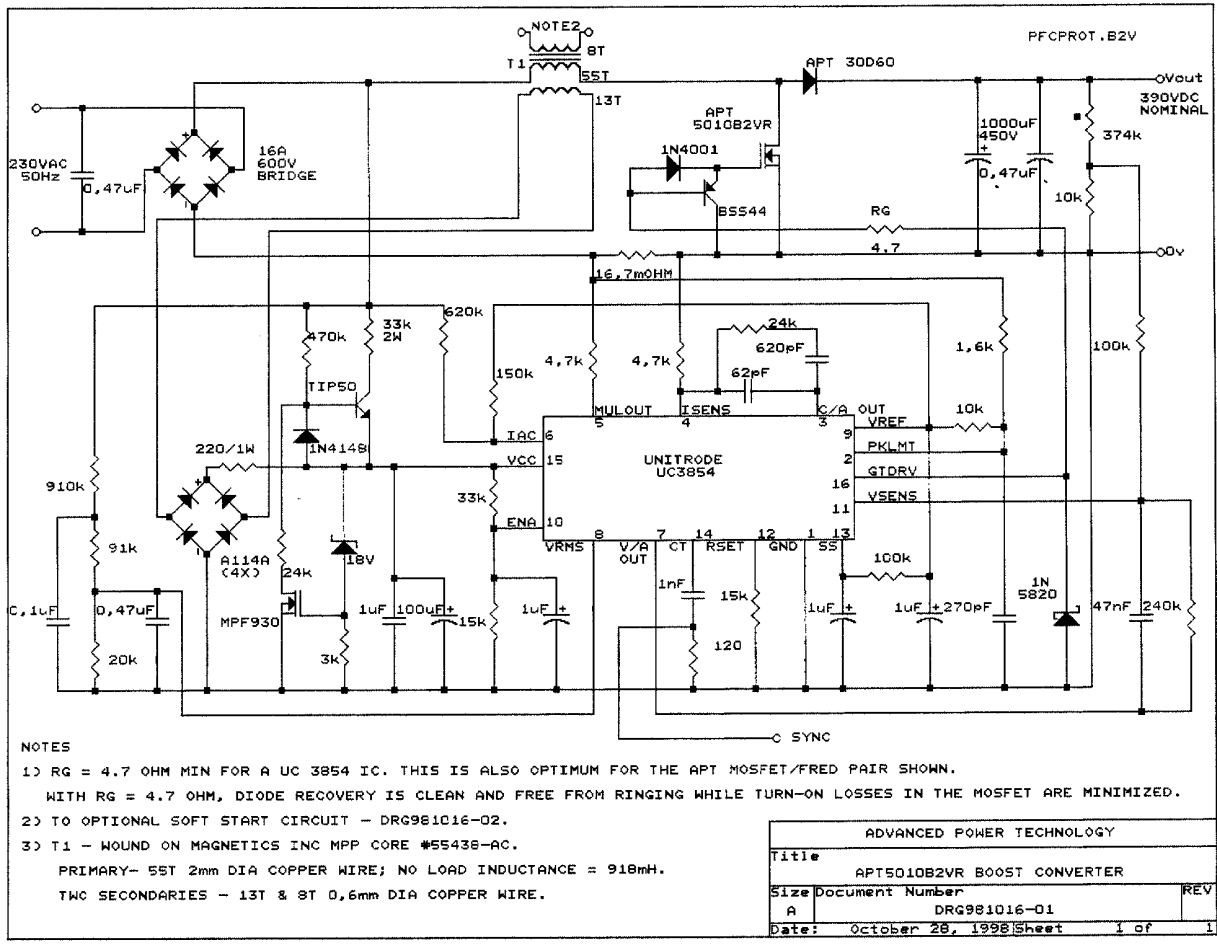
FIGURE 4. SCHEMATIC OF PFC TEST CIRCUIT

Heatsink thermal resistance was measured by energizing the series-connected rectifier bridge and MOSFET from the rectified and heavily filtered output of an arc-welding transformer. Heating current was regulated at 15A using the 16.7mΩ PFC sense resistor for source-feedback as shown in Figure 6.

After a 1hour stabilization run at an ambient temperature of 17.5°C, sink temperature under the MOSFET chip was measured at 71.5°C. DC voltages across the various elements were recorded:

V_{DS} (MOSFET) = 8.4V

V_F (diode #1) = 0.81V

V_F (diode #2) = 0.81V

I_{DC} = 15A (15mv across 1mΩ)

Whence P_{TOTAL} = 150.45W

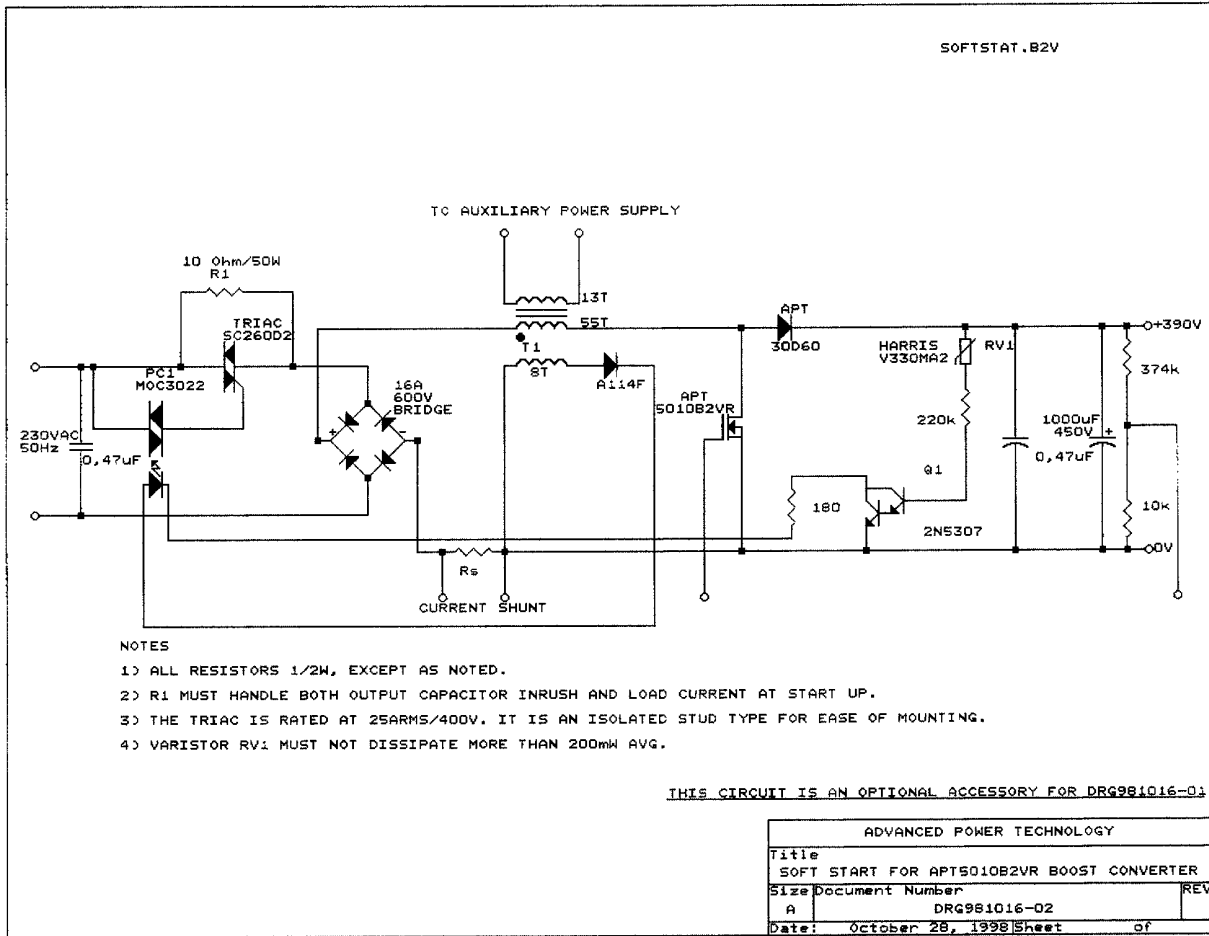And $R\theta_{SA} = \Delta T/ P_{TOTAL} = 0.36K/W$

FIGURE 5. SOFT START FOR PFC BOOST CONVERTER

It is of interest to speculate on the validity of this measurement, given that the distribution of "hot-spots"during calibration is not exactly the same as in an operating   PFC. With the exception of the boost diode, however, that dissipates significantly
when in use but remains inactive during calibration, the magnitude and distribution of the other losses are close to reality. By establishing the calibration current at 15A, very near to the 16ARMS 230VAC line current at 3.5kW output, bridge dissipation is approximately the same in both cases. Since it is known from prior art[4] that the overall efficiency of a continuous mode PFC operating at 3kW is about 95%, total semiconductor losses should lie between 100 and 150W. This is consistent

with the 150W dissipated in calibration. As for the diode "discrepancy", in an ISOTOP® the FRED chip is mounted on a common substrate with and so close to the FET that thermal transfer
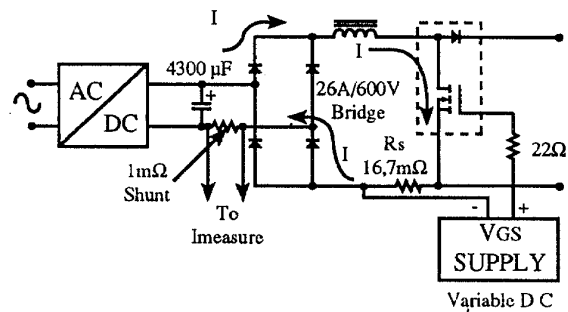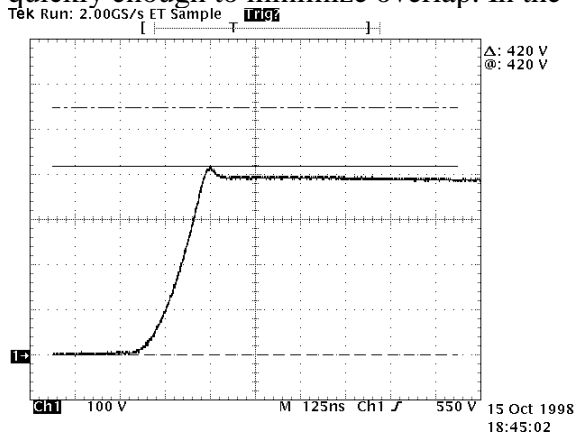

FIGURE 6. HEAT SINK
CALIBRATION

between module and sink is relatively independent of whether the heat is all MOS-generated as in calibration, or "multiplexed" between MOS and FRED as in a PFC.

It is evident that this latter presumption would not apply if the power circuit were assembled from three discrete components spaced apart on the heatsink. With three widely separated hot spots, heat
distribution would be less concentrated and heatsink effectiveness greatly enhanced. The possibility of excessive heat concentration should always be considered when designing with highly integrated power modules.

Gate Drive Optimization:

One of the key benchmarks in PFC design is to establish optimum gate drive for the MOSFET during turn-on and turn-off. While it is well established that overlap between drain-current-fall and drain-voltage-rise times at turn-off is a major contributor to switching losses, it is also known that most controller ICs are incapable of discharging the gate capacitance and absorbing the Miller current of a large die MOSFET quickly enough to minimize overlap. In the

circuit of Figure 4, the high-pulse-current PNP emitter follower connected between IC output and MOSFET gate effectively shorts the MOSFET gate to ground at turn-off, thereby eliminating this problem.

Comparative measurements show that when the circuit is operated at 2kW without the emitter follower, drain overlap increases from 50ns to 150ns and semiconductor losses rise from 53W to 86W. These higher losses could even precipitate thermal runaway, were the test circuit to be operated at full power without the PNP. Its use at the very highest power levels is therefore mandatory. Ironically, the much higher circuit di/dts produced by the emitter follower can also generate dangerously high voltage transients, unless great care is taken to minimize circuit stray inductance. MOSFET drain voltage and current waveforms with and without the PNP are illustrated in Figure 7.

References 1 and 2 show that for any given boost-diode technology there is a limited range of MOSFET turn-on di/dt that yields the best mix of low switching losses and near zero FRED-generated EMI.
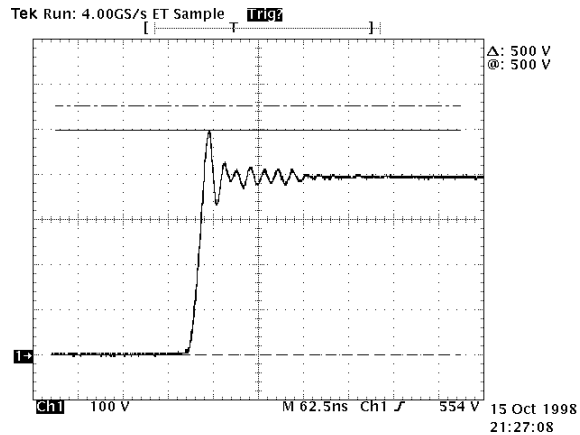
without emitter-follower   b) with emitter-follower
FIGURE 7. DRAIN-SOURCE TURN-OFF VOLTAGE

At elevated di/dt, peak recovery currents in the FRED are very high and cause excessive

switching losses in the MOSFET, while exacerbating any tendency for the FRED to

"snap ", that is for its peak recovery current to decay to zero so fast that the entire power circuit is shocked into oscillation. Should this occur, EMI becomes unmanageably high.

As the MOSFET is slowed down by gradually increasing R_G, peak recovery currents in the FRED diminish rapidly. Initially, the rate at which this occurs is high enough for losses in the MOSFET to actually decrease, despite the longer turn-on times. By the same token, any tendency for the circuit to ring is lessened. Eventually, though, the ever-longer MOSFET turn-on times predominate over the lower recovered energy in the FRED, and total losses begin to rise again. This indicates that

there is a range of R_G values where MOSFET turn-on losses are at or near a minimum, with EMI noise very low or non-existent. It cannot be over-emphasized, however, that the values of R_G so identified apply only to a specific combination of MOSFET and FRED, and will also depend heavily on physical layout of the power circuit.

Because APT FREDs are produced with an optimum diffusion profile, from high voltage epitaxial silicon and platinum heavy-metal minority-carrier lifetime control, they are characterized by exceptionally low reverse recovery currents at maximum temperature and rated current, and are not at all prone to "snap-off " during the final phase of recovery. In a boost converter the benefits accruing from this are substantially reduced losses in both MOSFET and FRED, and a higher degree of freedom in choosing the best value of R_G for optimal MOSFET turn-on. The recovery behavior of a FRED should always be evaluated at rated current and temperature, in that

performance data quoted at 25°C and with low test currents can be grossly misleading.

In a boost converter piloted by a UC3854, the risk that ringing between the MOSFET gate impedance and IC -driver might produce overvoltages across the driver imposes a 4.7Ω minimum value on R_G[5]. When this value is used in the circuit of Figure 4, the time constant resulting from 4.7Ω and the 500V/100mΩ MOSFET input capacitance yields a turn-on di/dt that is almost perfect for totally noise-free low-loss switching. Figure 8 illustrates the EMI-free nature of MOSFET turn-on into a 1500W load. Power output was limited to 1500W, because the 2 ½" long wire extension in the MOSFET drain link needed for the current probe adds too much stray inductance for safety at full power.

Voltage Overshoot at MOSFET Turn-off:

As emphasized already, for high overall system efficiency it is vital to minimize MOSFET switching losses by ensuring fastest possible turn-off. With the PNP emitter follower installed for this purpose, drain current transitions in the order of 1000A/µs are routine. While guaranteeing excellent efficiency, such transitions nonetheless exacerbate the effect of parasitic strays in the all-important MOSFET/FRED/output-capacitor loop. Assuming that the MOSFET will not be rated at more than 500V, based on a nominal 390VDC output and the need to limit R_{DS} (ON), the available margin for voltage overshoots is only110V.

By Lenz' Law:

$E = L_{STRAY}*di/dt$

$R_G = 4.7Ω$

$L=(110/1000)*10^{-6}$ Henry=110nHmax

Δ: 524 V
@: 524 V

A1▶

Ch1   100 V   M 25.0ns Ax1 ⌐   26.2 A   15 Oct 1998
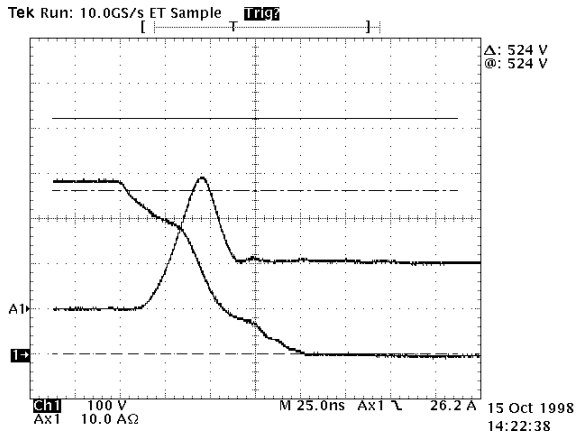Ax1   10.0 AΩ   14:22:38

FIGURE 8. MOSFET TURN-ON

In conventional point-to-point wiring of discrete power components, such low values of loop inductance are not easy to attain. Just a few centimeters of hook-up wire will suffice. Although inductive strays may be reduced somewhat by using stripline links between the filter
capacitor and the two semiconductors, overshoots during steady-state operation at full output may still be dangerously high. To alleviate this, the loop inductance must be reduced yet more.
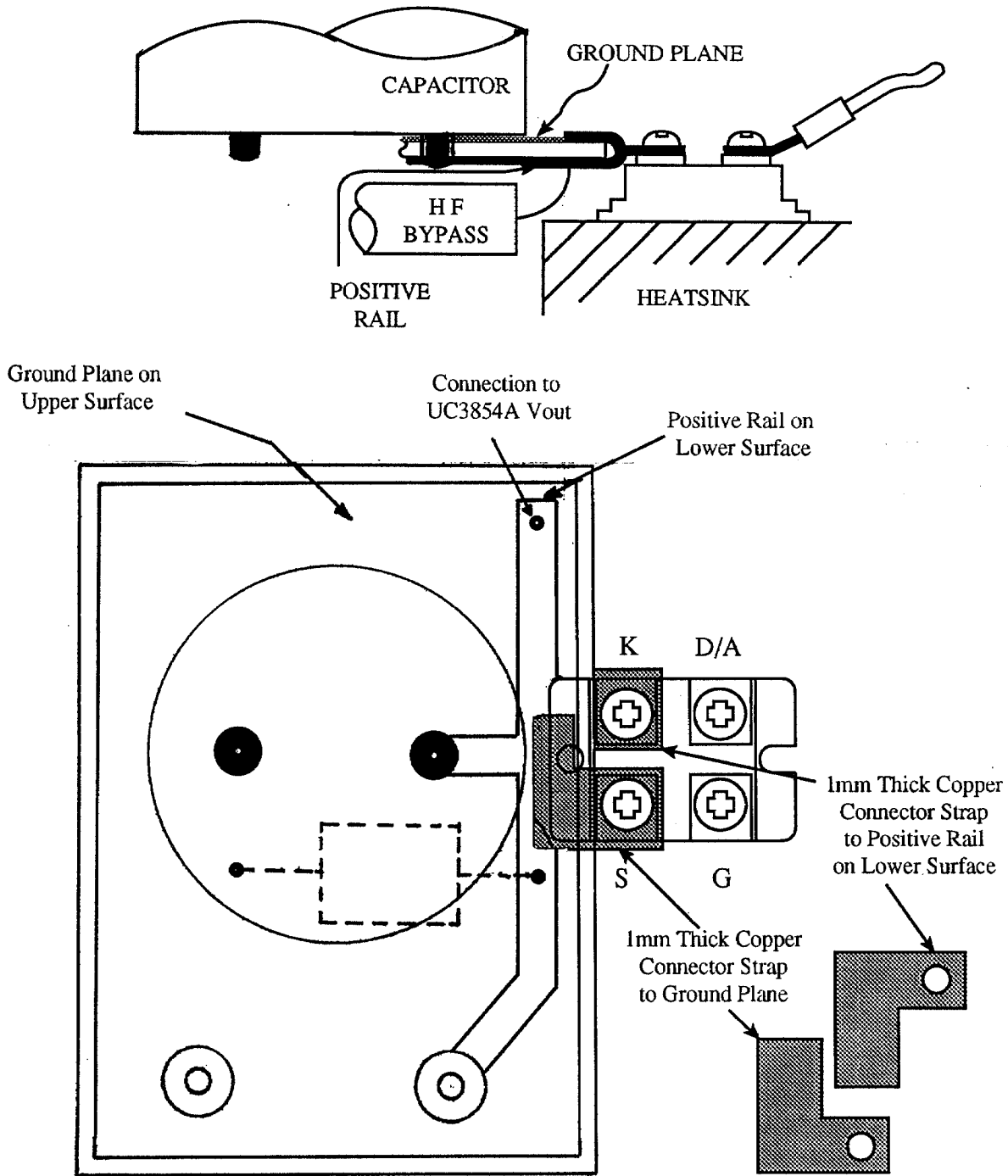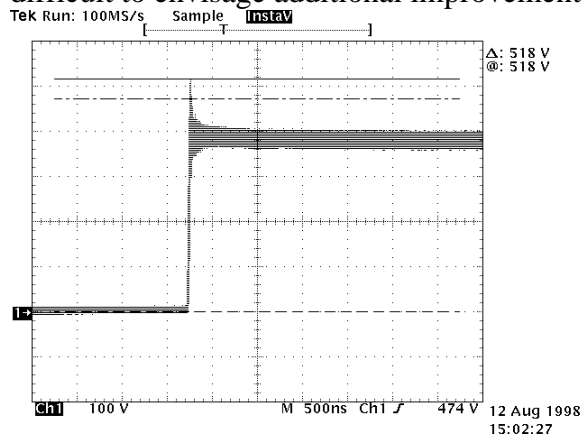
FIGURE 9. ISOTOP® TO FILTER CAPACITOR LINK

Since physical layout is largely dictated by the size and location of the filter board relative to the heatsink mounted semiconductors, a means must be found first to non-inductively couple the two semiconductor chips together and then to non-inductively connect this pair to the capacitor. An ISOTOP® packaged PFC module is ideal for this purpose; 5-10nH chip-to-terminal strays facilitate low inductance internal connections, while top-surface located screw terminals permit direct liaison to a double-side-metalled filter board via short copper straps. PFCs based on this concept, illustrated in Figure 9, can easily deliver the full 3.5kW allowed from European 230V/16A single phase mains without stressing the MOSFET beyond 500V during normal operation, although peak voltages may exceed this briefly at power-up. In the US, output power is limited to around 3.2kW by the 15ARMS fuses associated with 230V two-phase mains. When run from 120V single-phase mains, available power will be somewhat less than 1500W, because of the increased circuit losses at low input voltages.

In a well-conceived PFC laid out with with low inductance interconnects and optimized semiconductors, it is reasonable to suppose that a good part of the residual overshoot is generated by ESL in the filter capacitor and related hardware. As a consequence, it is difficult to envisage additional improvement without resorting to RC snubbers or similar protective devices. It is also clear that any PFC assembled from discrete semiconductors, with their higher strays, will always generate higher overshoots than a specialist module like the ISOTOP®. On the positive side, a discrete component assembly is generally less expensive to build, and as long as the higher overshoots do not generate unsustainable avalanche power, can be an attractive alternative to modules in cost-sensitive applications.

Circuit Performance:

1) The APT5010JVRU2 ISOTOP®-equipped test assembly was evaluated under the following conditions:
$T_A = 27°C$ (after ½ hour run time)
$R_L = 39Ω$ (hot)
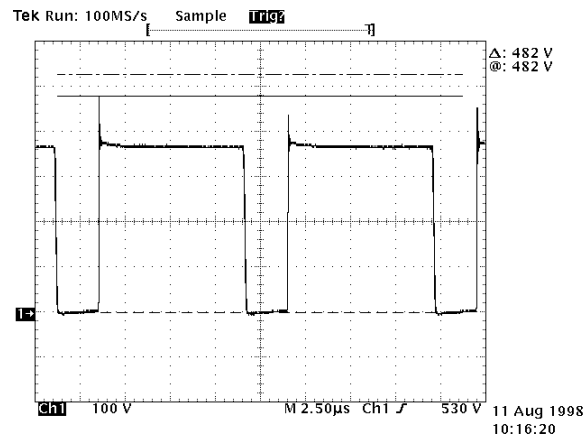Recorded results were:
$V_{AC} = 218VRMS$ (at bridge input)
$I_{AC} = 16.2ARMS$,
$V_L = 361VDC$ (361VRMS),
$T_S = 73°C$
I_{AC} was measured with a Tektronix #520B oscilloscope and Pearson # 411 current transformer.
V_{AC}, V_L and R_L were measured with an HP #973A true-RMS DVM.
T_S was measured with an AOIP platinum resistance digital thermometer.

a) start-up

b) steady-state

FIGURE 10. DRAIN VOLTAGE AT TURN-OFF, APT5010JVRU2

From these data:
$P_{OUT}=V_L^2/R_L=3342W$, $\Delta T_{SA}=46°C$
Losses in the PFC semiconductors:
$P_{SC}=\Delta T_{SA} / R\theta_{SA}=46/0.36=128W$
Input power:
$P_{IN}=(V_{AC}x\ I_{AC})=(218x16.2)=3532W$
Soft start losses:
$P_{SS}=14$ W at 16.2ARMS (from SC265 triac data sheet)
Efficiency, excluding soft start losses:
$\eta=P_{OUT}/(P_{IN}-P_{SS}) = 3342/ (3532 -14)$
$= 95\%$
As portrayed in Figures 10a and b, peak overshoot voltage at the MOSFET drain does slightly exceed 500V at start-up, but during normal operation stabilizes at a very safe 482V. In the unlikely event that startup transients ever drove the MOSFET briefly into avalanche, no harm would result as long as the total power rating of the device was respected. APT's Power MOS V® process is optimized to allow safe operation in repetitive avalanche.

2) The PFC test assembly was next evaluated with an APT5010LVR TO-264 packaged MOSFET and TO-247 packaged APT30D60B FRED replacing the single ISOTOP®. The MOSFET was mounted in the same position as the module, with the FRED alongside. Stray inductance in the MOSFET/FRED/filter capacitor loop was minimized by using pseudo-stripline interconnects. As a first step, a full power 3.5kW run was made with the MOSFET attached to the heatsink with an M3 machine screw torqued to 6dNm. Isolation was provided by a 0.6mm thick aluminum nitride shim coated on both faces with Thermalcote II non-silicone grease. The FRED was similarly mounted, but with a Bergquist "Silpad"shim replacing the AlN, this material being adequate for the modest amount of heat generated by the FRED.
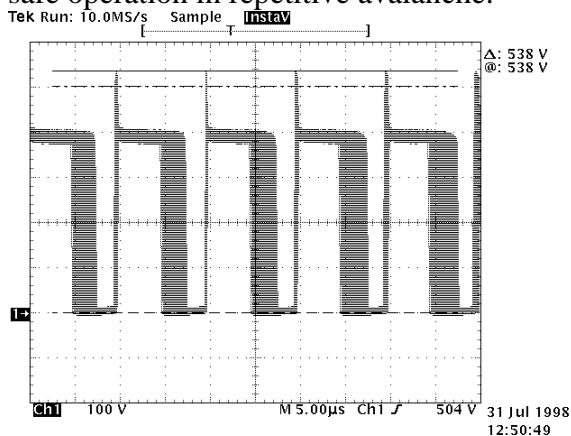
a) start-up
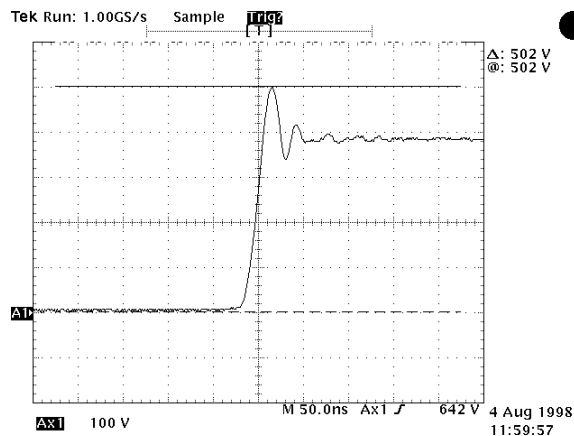
b) steady-state

FIGURE 11. DRAIN VOLTAGE AT TURN-OFF, APT5010LVR

Test conditions were:
$T_A= 24°c$ (after ½ hour run time)
$R_L = 39\Omega$ (hot)
Recorded results were:
$V_{AC}= 218VRMS$

$I_{AC} =16.3ARMS$
$V_L=360VDC$ (360VRMS)
$T_S = 69°C$
From these data:
$P_{OUT}=3342W$, $\Delta T_{SA}=45°C$

Losses in the PFC Semiconductors:
$P_{SC} = \Delta_{SA} / R\theta_{SA} = 45/0.36 = 125W$
Soft start losses:
$P_{SS} = 14W$
Input power:
$P_{IN} = (218 \times 16.3) = 3553W$
Efficiency, excluding soft start losses:
$\eta = 3342/(3553 - 14) = 94\%$

Comparing this performance with that of the ISOTOP® shows that the two approaches yield virtually identical results, at least where thermal response and efficiency are concerned. This is not surprising in
that both have the same size MOSFET featuring similar junction-to-sink thermal resistances. The FRED is located on the sink close enough to the FET to ensure roughly the same heat distribution.

Overvoltage behavior, however, is not at all comparable. Figures 11a and b depict MOSFET drain voltage waveforms at power-up and in the steady-state. Start-up transients peak at 538V instead of 518V, while the steady-state overshoots stabilize at 502V rather than 482V. The risk of repetitive avalanche with its high losses is substantially increased with the discrete solution.

3) The test assembly was next modified to allow spring-clip rather than M3 screw attachment of the TO-264 package. The clip applied a force of approximately 5kg between the FET and its sink, centered over the silicon chip. A full-load run was then made with the same conditions as before:
$T_A = 24°C$ (after ½ hour run time)
$R_L = 39\Omega$

The recorded results from this run were not quite as expected, in that the heatsink temperature (T_S) rose 3°C to 72°C. Input and output voltages and currents were unchanged from the previous run.

The most plausible explanation for this apparent increase in sink temperature is the improved thermal contact made possible by the clip. With the clip, close and homogeneous contact between semiconductor and sink is assured by the centrally applied mounting force. With screw mounting, good contact is invariably limited to a relatively small area close to and around the mounting screw. Away from the screw, the contact tends to degrade progressively due to package "tilting", this being exacerbated by the presence of any resilient isolating medium[6]. Because most of the heat is then transferred to the sink through a relatively small area not directly under the heat source, case to sink thermal resistance is increased and junction temperature rises. The lower sink temperature measured with the screw mount reflects poor heat transfer directly under the chip. Were the temperature probe to be moved nearer the screw, the measured sink temperature would rise. In that higher junction temperatures lead to more losses and degraded reliability, it is evident that clip mounting is preferable.

4) From the above it is fairly evident that clip-attached packages outperform their screw-mounted brethren. In a pressure-mounted design, mounting holes are un-necessary and their suppression shrinks size, reduces cost and improves performance. The T-MAX™ from APT is such a design. Featuring the same footprint as a TO-247, this clip-mount design accommodates the same size chips as those in the larger more costly TO-264s. An APT5010B2VR T-MAX™ equivalent to the TO-264 5010LVR was tried in the test circuit. Test conditons were:
$T_A = 25°C$ (after ½ hour run time)
$R_L = 39\Omega$
Recorded results were:
$V_{AC} = 218VRMS$
$I_{AC} = 16.2ARMS$
$V_L = 361VDC$ (361VRMS)
$T_S = 74°C$

From these data:

$P_{OUT} = 3341W$

$\Delta T_{SA} = 49°C$

Losses in the PFC semiconductors:

$P_{SC} = \Delta_{SA} / R\theta_{SA} = 49/0.36 = 136W$

Input power:

$P_{IN} = (218 \times 16.2) = 3532W$

Softstart losses:

$P_{SS} = 14W$

Efficiency, excluding soft start:

$\eta = 3341 / (3532 - 14) = 95\%$

During this final test, MOSFET drain voltage waveforms were found to be comparable to those from the TO-264. This is to be expected in that the physical layout of the two variants is very similar.

Figure 12 is an oscillogram of the 230VAC 50Hertz mains current at 3500W out, and shows that the line harmonics at 16ARMS are well within the limits prescribed by IEC 1003-2.

Conclusions:

In the design of very high power PFC circuits the proper choice of power components, the optimization of MOSFET switching speeds and the mechanical layout of the output power loop are equally important to success. The selection of a low on-resistance MOSFET matched to a fast/soft-recovery FRED is the first step to achieving high efficiency with low EMI. The gate circuitry must then be tailored to drive the MOSFET/FRED pair for minimum switching losses and acceptable EMI. Finally, the MOSFET/ FRED/ output capacitor power loop must be laid out to minimize overshoot-producing stray inductance. It has been demonstrated that use of an ISOTOP®-packaged PFC module, incorporating APT's state-of-the-art Power MOS V® and FRED technologies, enables full authorized power to be drawn from

either European (3500W) or North American (3200W) 230VAC mains at 95% efficiency, with safe snubberless operation of the power devices.

In situations where cost and/or mechanical considerations preclude use of a module, nearly the same performance is available from either a TO-264 or a T-MAX™ packaged MOSFET plus TO-247 discrete FRED. Should a TO-264 be preferred over the T-MAX™, it is shown that superior thermal performance is obtained by spring-clip mounting rather than with a screw. When either of these discrete products is paired with a FRED to replace the module, the unavoidable increase in stray inductance generates voltage overshoots across the MOSFET that just exceed 500V in the steady state, more during power-up. Because Power MOS V® technology allows safe operation in avalanche, no harm will result as long as total power dissipation ratings are respected.
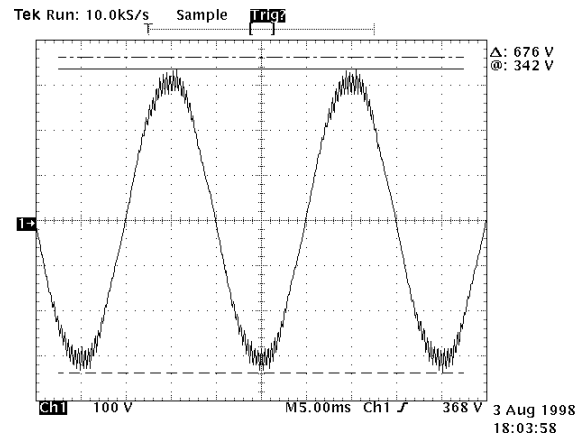
FIGURE 12. 230VAC MAINS CURRENT 3500W LOAD

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