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APPLICATION NOTE

UNDERSTANDING THE DIFFERENCES BETWEEN STANDARD MOSFETs AND AVALANCHE ENERGY RATED MOSFETs

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UNDERSTANDING THE DIFFERENCES BETWEEN STANDARD MOSFETS AND AVALANCHE ENERGY RATED MOSFETS

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Abstract

Avalanche rated MOSFETs were introduced in the mid '80s amid great controversy. Some misleading information about the avalanche energy rating was circulated during this period and to this day misunderstanding persists. Many circuit designers consider the avalanche energy rating as a figure of merit and do not consider the tradeoffs they are making with input capacitance and gate ruggedness. This paper will dispel some of the misinformation, clarify the need for avalanche energy rated MOSFETs and present the tradeoffs between rated and non rated devices.

Failure of a power MOSFET in the avalanche mode results from forward biasing the base emitter junction of the parasitic NPN transistor, turning it on. The turn-on of the NPN transistor is influenced by defects, current density, junction temperature and the quality of the base-emitter short. Device structural changes to prevent the NPN from turning on, are presented.

Once the MOSFET structure has been optimized the avalanche rating becomes a matter of guaranteeing high current avalanche operation at maximum operating junction temperature. This is done using the single pulse avalanche energy (W_{AS}) test/rating. The W_{AS} test is designed to test the device at full rated operating junction temperature and high current density. An example of how to calculate the W_{AS} rating from the transient thermal impedance curve is presented.

While verifying the junction temperature of a device during the W_{AS} test it was found that the temperature was higher than predicted. It was determined that the transient thermal impedance curve generated using forward conduction losses as the heat source was not the same as a transient thermal impedance curve generated using avalanche energy as the heat source. Forward conduction and avalanche energy generated transient thermal impedance curve are presented.

Introduction

In 1985 General Electric (GE) introduced the first avalanche rated power MOSFET devices. This

introduction was followed by a split of the power MOSFET manufacturer's into two camps. One camp followed GE's lead and introduced their own version of "rugged" devices and the others

proceeded to argue why the industry should not adopt the avalanche rating as a device specification.

The main argument for ruggedness was, it is impossible to totally eliminate all voltage spikes in high power electronic equipment and rugged devices were necessary to eliminate the accidental over voltage of the power devices in the circuit. It then followed that if the fear of damage, of the power device, from over voltage was eliminated the designer could reduce cost by eliminating unnecessary components, such as snubbers, transient suppressers, etc., and operate closer to the breakdown voltage of the device.

The main argument against the avalanche rating was, if the designer was given an avalanche rating he would assume it was okay to operate the device in a repetitive avalanche mode and would eliminate necessary components such as snubbers, transient suppressers, etc. with the result of reduced reliability. The opponents were also concerned their maybe a wear out mechanism associated with long term repetitive avalanche operation and there was insufficient long term studies to determine if this was the case.

The market has proven the proponents of avalanche rated devices to be correct as many users require an avalanche rating be provided and most manufacturers now offer avalanche rated devices. Time has also eliminated the fear of using Power MOSFET in the repetitive avalanche mode as no wear out mechanism has been identified.

Avalanche Failure Mechanisms

When a power MOSFET is in the off-state or

operated in saturation the drain-source voltage is supported across the body-drain P-N junction. If the device is subjected to a voltage in excess of it's breakdown voltage the electric field across the P-N junction will reach a value at which avalanche multiplication will commence. Computer modeling has shown that the maximum electric field occurs on the corner of the P diffusion resulting in most of the avalanche current entering the body at this point and flowing under the N+ source diffusion (arrow Figure 1) to the source metal contact. The lighter doped P- region constitutes a resistance (r_b') which will give rise to a voltage drop beneath the N+ diffusion. The P-N junction formed by the body and source diffusions is the base-emitter junction of a parasitic NPN transistor. If the resistance is

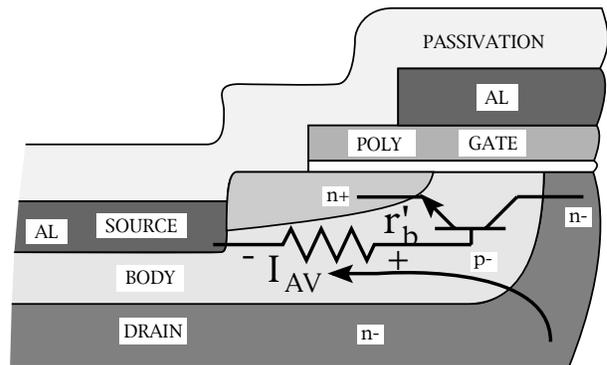


Figure 1. Cross Section of an APT MOSFET Showing the Parasitic NPN Transistor

too large or the avalanche current high enough the P-N junction will become forward biased turning the bipolar transistor on. Due to non uniformity's in the diffusions, the negative temperature coefficient of the voltage associated with a forward biased P-N junction and the heat generated by the energy from the avalanche current, current crowding will rapidly ensue with the likely result of second

breakdown of the parasitic transistor and failure of the device. If the design or the manufacturing process does not create a uniform structure or if defects are present in the silicon the point(s) of avalanche will be a localized event giving rise to high avalanche current density at these points causing a relatively large potential drop across r_b , sufficient to forward bias the P-N junction and hence activate the parasitic NPN bipolar transistor causing failure.

Definition of Ruggedness

When applied to a power MOSFET the term “Ruggedness” describes the ability of that device to survive operation in the avalanche mode at a specified current and junction temperature. The avalanche voltage is determined by the physical and electrical characteristics of the silicon starting material, the avalanche current being forced and the junction temperature. The specified avalanche current is usually the continuous current rating of the device as in a practical application the peak operating current of the device will typically be about the continuous current rating after thermal considerations and proper derating has been applied. The junction temperature is usually rated at the maximum operating junction temperature of 150°C.

Avalanche Ratings

There are three specifications on the data sheet relating to avalanche: 1.) The maximum avalanche current rating, which gives the maximum allowable current that the device can be subjected to in the avalanche mode, either repetitive or non repetitive, up to a junction temperature of 150°C. This is the

most important specification as it is the definition of ruggedness presented in the previous section. 2.) The repetitive avalanche energy rating, which gives the maximum allowable energy per pulse which the device can be subjected to on a repetitive basis. This specification is somewhat trivial in the since that if one were to use a typical device with repetitive avalanche energy pulses at 100kHz at the repetitive avalanche energy rating of say 20mJ the resulting power losses would be 2000W which of course is unrealistic. However, as the name implies one can subject the device to avalanche on a repetitive basis as long as the maximum junction temperature of 150°C is not exceeded. 3.) The third rating is the non repetitive avalanche energy rating, which gives the maximum avalanche energy the device can handle in a single pulse with a starting junction temperature of 25°C. The single pulse rating implies the device can be used as a transient voltage suppresser and indeed it could be. However, the MOSFET is too expensive a device to be used in this way and most transient suppression applications are not well controlled and require peak current far in excess of the continuous rating of a typical MOSFET. The single pulse avalanche energy specification actually provides the user with information on test conditions which the device is subjected to during testing to insure the device is capable of surviving an avalanche pulse at rated current at 150°C. It can also be used as test conditions by the user to verify the device avalanche capability.

Since the single pulse avalanche energy rating is given in Joules, many users are under the misconception that energy is the avalanche failure mechanism. The preceding discussion on failure

mechanisms and definitions did not even mention energy as being part of the failure mechanism. In fact the only function the energy performs in the single pulse test is the heating of the junction. A 1000V, 11Amp MOSFET being avalanched at 1mA for 10 seconds will not fail even though the device is being subjected to over 10 Joules (Watt-seconds) of energy. In fact with proper heat sinking there would be very little junction temperature rise during the test. Therefore, it must be understood that the failure mechanism is the combination of junction temperature and avalanche current not energy.

Avalanche Testing

To be an effective test of the suitability of a MOSFET to be rated as “Rugged” the test must guarantee the criteria set forth in the section defining Ruggedness. That is, the device must survive operation in the avalanche mode at it’s continuous current rating at a junction temperature of 150°C. It seems simple enough to heat the device to 150°C and force a current equal to the continuous current rating of the device from a current source capable of an output voltage in excess of the breakdown voltage of the device. In fact some engineering and characterization testing is done in this manner. The problem with this method is the pulse must be a very short duration to avoid excessive heating of the junction due to the very high power levels achieved during the test. For instance a 500V, 23Amp device will reach more than 11,500W peak power during the avalanche test and if the test lasts for 10µsec the resulting junction heating would be in excess of 40°C. A slight variation to this test method is to start with a junction temperature of 25°C and use the energy generated during the test to self heat the device under test to the required

150°C junction temperature. One problem with this test is to determine how long the current pulse must be applied to the device to achieve the required 150°C junction temperature. To start, the breakdown voltage of a given population of devices of a particular type may have a breakdown voltage spread of as much as 20%, making the power applied at a given current vary as much as 20%. Also the power will increase during the test as the avalanche voltage will increase as the junction temperature rises. It is possible, with today’s microprocessor technology, to monitor, multiply and sum the instantaneous current and voltage at regular intervals to obtain the total energy into the device at any point in time. Dividing the total energy by the total time elapsed, to obtain the average power, and multiplying by the transient thermal impedance would give the junction temperature after any interval of time.

$$T_J = \frac{W_{AV}}{t_{AV}} \times Z_{\theta JC} \quad (1)$$

The equipment required for this type of tester would be very sophisticated and very expensive.

A variation of the above test method, relying on the stored energy in an inductor to control the junction temperature rise, offers a simpler less, expensive approach to the test. A simplified circuit used for this test with the associated current and voltage wave forms are shown in figures 2 and 3. This test method is appropriately referred to as Unclamped Inductive Switching (UIS) as there is no diode clamp across the coil to limit the flyback voltage appearing at the drain.

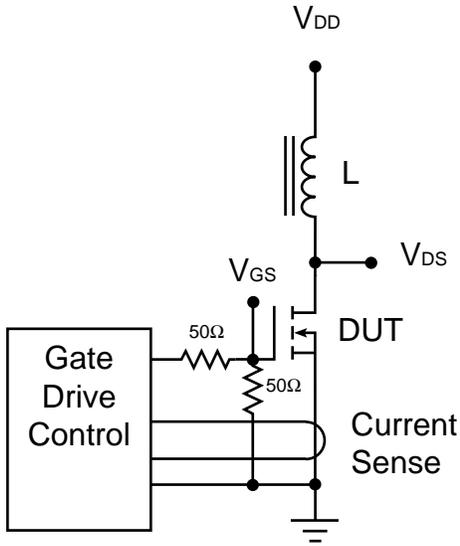


Figure 2. Simplified UIS Test Circuit

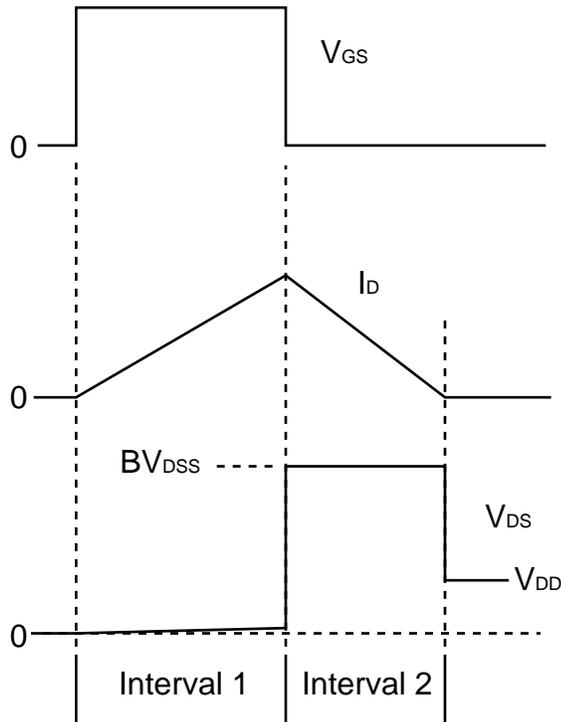


Figure 3. Waveforms Associated with Circuit in Figure 2

The DUT is turned on at the beginning of interval 1

causing the current in the inductor to increase at a linear rate. The inductor current increases until the desired peak avalanche current level is reached at which time the control circuitry will turn the DUT off ending interval 1. The amount of energy stored in the inductor is calculated from the equation:

$$W_L = \frac{1}{2}L \times I_D^2 \quad (2)$$

where:

W_L is the stored energy in the inductor in Joules, L is the storage inductor in Henrys, I_D is the peak drain current at the end of the charge interval 1 in Amp. This energy determines the junction temperature rise and can be calculated using equation 1.

Interval 2 begins at the end of interval 1 as the DUT is turning off interrupting the charging of the inductor. Since the inductor current cannot change instantaneously, the stored energy in the inductor will cause the drain-source voltage to rise rapidly until the drain-source breakdown voltage is reached. The DUT will remain in breakdown until all of the energy in the inductor is dissipated. The energy dissipated can be calculated from the equation:

$$W_{AV} = \frac{1}{2}L \times I_D^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \quad (3)$$

where:

W_{AV} is the energy dissipated in the DUT during avalanche in Joules, $\frac{1}{2}L \times I_D^2$ is the energy stored

in the inductor and $\frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$ is an adjustment

factor to account for the amount of energy contributed by the charging voltage supply during

avalanche interval 2.

Figure 4 shows a modification to the test circuit that simplifies the energy calculation and makes the test independent of the charging supply voltage V_{DD} . The series switch in the charging voltage supply applies the charging voltage to the inductor at the beginning of interval 1 and to remove it at the end of interval 1. The diode clamps the inductor to ground during interval 2. This makes the energy stored in the inductor and the energy dissipated in the DUT during avalanche the same and is calculated using equation 2.

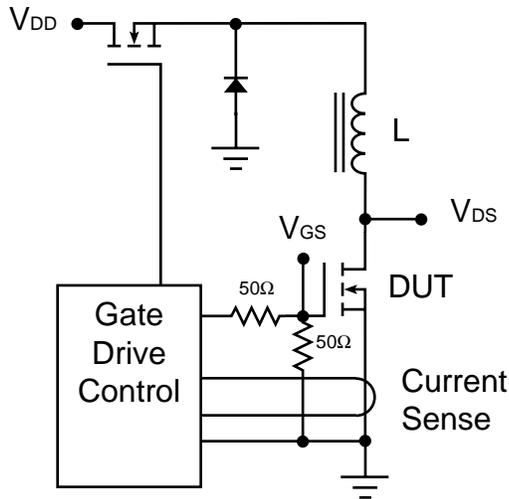


Figure 4. Modified UIS Test Circuit

Single Pulse Avalanche Energy Rating

Using the last test circuit described in the previous section the amount of energy needed to raise the junction temperature to 150°C from 25°C is calculated using the average power dissipated by the device during avalanche and the transient thermal impedance curve. First we must determine the

power which is dissipated by the DUT if a rectangular current pulse were applied to the device at a test current equal to the continuous current rating of the device. Power during avalanche is:

$$P_{AV} = I_D \times BV_{DSS} \quad (4)$$

where:

P_{AV} is the power dissipated in Watts,
 I_D is the drain current in Amps and BV_{DSS} is the breakdown Voltage in Volts.

For an APT5025BN, 500V, 23Amp P_{AV} would be:

$$P_{AV} = 23 \times 500 = 11,500\text{W}$$

Knowing the power level generated and the requirement to raise the junction temperature by 125°C ($150-25$) during the avalanche test we can calculate a transient thermal impedance relating to these conditions:

$$z_{\theta JC} = \frac{\Delta T_J}{P_{AV}} = \frac{125}{11500} = 0.011^{\circ}\text{C}/\text{W}$$

From Figure 5, the transient thermal impedance curve published on the APT5025BN data sheet, time in avalanche necessary to raise the junction temperature 125°C with a rectangular power pulse of 11,500W would be $400\mu\text{sec}$ and the resulting avalanche energy required would be:

$$W_{AV} = P_{AV} \times t_{AV} = 11,500 \times 400 \times 10^{-6}$$

$$W_{AV} = 4,600\text{mJ}$$

Where:

t_{AV} is the time in avalanche in seconds.

Avalanche testing conducted at this calculated energy level showed the junction temperature was exceeding the 150°C calculated maximum by a great amount and comparison of specifications of similar devices on the market indicated this energy level to be unrealistic.

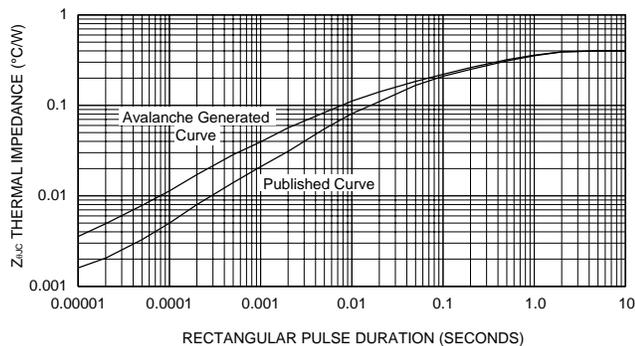


Figure 5. Transient Thermal Impedance Curve APT5025BN

Since the published transient thermal impedance curve is generated using forward conduction losses as the self heating mechanism and the temperature monitoring parameter is the body diode it was hypothesized that the curve maybe different if generated using avalanche energy as the self heating mechanism and breakdown voltage is used as the temperature monitoring parameter. A test fixture was constructed to generate a transient thermal curve using avalanche energy as the heat source. The results, shown in figure 5, were as hypothesized.

The time in avalanche was recalculated using the new transient thermal curve to be 105µsec and the calculated avalanche energy needed was 1210mJ. This agreed with subsequent avalanche testing as the maximum junction temperature ranged around the required 150°C.

Ruggedizing the MOSFET

In order that a power MOSFET may survive transitory excursions into avalanche it is necessary to manufacture a device with a uniform structure, free from defects throughout the crystal and that within the structure the resistance r_b' beneath the N+ should be kept to a minimum. In this way the chance of forward biasing the P-N junction is minimized.

As the epitaxial material is purchased defects in the epi are controlled at the time of manufacture by the epi manufacturer. Defects which maybe introduced during processing are controlled by the MOSFET manufacture by having a factory free from contaminants and using quality materials during the manufacture. The uniform structure is obtained during the design stage where careful attention is given to the layout of the chip.

The resistance r_b' beneath the N+ diffusion is reduced by increasing the carrier concentration of the P- region of the body diffusion. In addition to reducing r_b' beneath the N+ diffusion another result of the increased carrier concentration is an increase in the gate threshold voltage to a point above the maximum specification. To offset the increase in threshold voltage the gate oxide thickness must be reduced to lower the threshold voltage within the specification range of 2 to 4V. A result of thinning the gate oxide is an increase in input capacitance and a reduction of the gate oxide rupture voltage.

The increase in capacitance and resulting increase in gate drive requirements and a gate more sensitive to ESD are the compromises the designer must make

when specifying an avalanche rated MOSFET over a non avalanche rated MOSFET. For example an APT5025BN non avalanche rated MOSFET has a typical input capacitance C_{ISS} of 2380pF, a maximum total gate charge Q_g of 130nC and a continuous maximum gate voltage rating of 30V. Where an APT5025BNR avalanche rated device has a typical input capacitance C_{ISS} of 3950pF, a typical total gate charge Q_g of 220nC and a continuous maximum gate voltage rating of only 20V. The increase in capacitance is a substantial 66% and the resulting gate charge increase is 70%.

Conclusions:

Specifying an avalanche rated MOSFET into a circuit which does not require it comes with a penalty. A better solution would be careful attention to PC board layout, transformer design and the addition of an expensive snubber to prevent over voltage spikes. This solution will result in a more reliable, more efficient and possibly less expensive system.



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